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Beyond CMOS computing with spin and polarization

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Spintronic and multiferroic systems are leading candidates for achieving attojoule-class logic gates for computing, thereby enabling the continuation of Moore's law for transistor scaling. However, shifting the materials focus of computing towards oxides and topological materials requires a holistic approach addressing energy, stochasticity and complexity.

Computing efficiency has made exponential gains over the past five decades stemming directly from size scaling, technological breakthroughs in the control of transport in semiconductors[1], lithography[2] and the success of von Neumann computing architectures[3]. The cornerstones of transistor size scaling are Moore's law[4] and Dennard's scaling[5], which have led to a reduction in transistor costs[4], shrinking of the circuit area[5], lowering of the supply voltage, and growth of complexity and parallelism in the computer architecture[3] — scaling of nanoelectronics based on complementary metal–oxide–semiconductor (CMOS) transistors is now approaching a characteristic size of 10 nm (ref. [1]). In the past 15 years, however, scaling has deviated from Dennard's trend, which states that the power density of circuits stays roughly the same as transistors gets smaller, concurrent with voltage reductions. And Moore's law, which is the observation that the number of transistors on integrated circuits approximately doubles every two years, has relied increasingly on material advances to enhance the mobility[6,7] along with metal-gate electrode and high-k dielectrics in order to improve the electrostatic control of carriers in 3D transistors[8].

To make significant improvements in the energy efficiency and speed of integrated circuits in the future, the continuation of Moore's law scaling will require the introduction of non-traditional materials and structures, as well as beyond-CMOS logic devices[6,9–13] that are based on quantum nanoelectronic or nanomagnetic principles. The introduction of new state variables — physical quantities that store and transmit the logic state — for computing, interconnects and memory, such as electron dipole, spin, orbital state and light intensity/helicity, is one way to continue Moore's law scaling. This is a revolutionary materials approach to continuing Moore's law, where new materials and physical phenomena are utilized for enabling fundamentally better computing devices at the physical layer. In particular, computing with spintronics/multiferroics is emerging as a leading candidate for memory and logic[9–13].

Central to the need for a device technology beyond CMOS is an effect known as the Boltzmann tyranny[14] — this is a consequence of the thermal energy distribution of electrons/holes at room temperature, in any device that is switched by modulating charge conductivity by an energy barrier. It dictates that the ratio of on-current and off-current in a device is related to the voltage swing, and thus it prevents the supply voltage of high-performance CMOS devices from going below ~0.5 V (ref. [3]). While new materials, such as III–V semiconductors and two-dimensional materials, have promising characteristics of improved carrier transport and reduced dynamic energy, they are still subject to Boltzmann tyranny and can at best be a continuation of the existing CMOS scaling trend. In contrast, new state variables for computing, interconnects and memory can provide a break from this paradigm, relying on order parameters such as polarization, magnetization and strain, which exhibit collective switching, strong thresholding behaviour and non-volatility. It is also possible to circumvent Boltzmann tyranny with tunnelling field-effect transistors (TFETs)[9], where the tunnelling transport physics allows for under 60 mV per decade current modulation.

In this Perspective, we describe a path for computing with spintronic and multiferroic devices, and discuss the milestones that need to be surpassed for enabling this transition. We first define a beyond-CMOS collective switch in terms of the reversal of a material's order parameter (Θ to $-\Theta$) — defining a metric for the energy required for switching (E_{sw}), which is related to the stored energy of the order parameter ($E(\Theta)$). Second, we consider the minimal energy and voltages that are required for transmitting a logic variable on an interconnect from the point of view of the thermodynamic limits given by photonic/electronic shot noises[15,16]. This new perspective enables a definition of the key milestones for spintronics/multiferroics computing, which can be viewed as experimental grand challenges. We identify experimental targets for magnetization switching efficiency, detection of the state of the magnet, and interconnects for spintronics. We also propose the holistic paradigm of energy scaling, error rate scaling and complexity scaling for new computational devices, non-traditional/neuromorphic architectures and new computing techniques, such as stochastic[17–20] and Shannon-inspired computing[18].

A collective switch

We restate the concept of a beyond-CMOS switch as a collective switch that reverses a materials order parameter (Θ). Examples of order parameters from Landau's theory are magnetization ($\mathbf{M}$), antiferromagnetic order (L), polarization ($\mathbf{P}$), and strain ($\boldsymbol{\sigma}$). A collective switch is a device that reverses this order parameter in a volume of the material (Fig. 1a) in a manner that allows for nonlinear input–output transfer characteristics. The collective switch exhibits a nonlinear transition when the input exceeds a threshold. The switch must transduce the state variable to carry a logic signal η and couple to an interconnect (Fig. 1b), which carries the signal to the next stage of the logic circuit. The switch must also respond to an input logic signal η from the previous circuit stage to reversibly change the sign of the order parameter.

The thermal stability of the switch is given by the value of the retention energy barrier (ΔE) obtained from the dependence of

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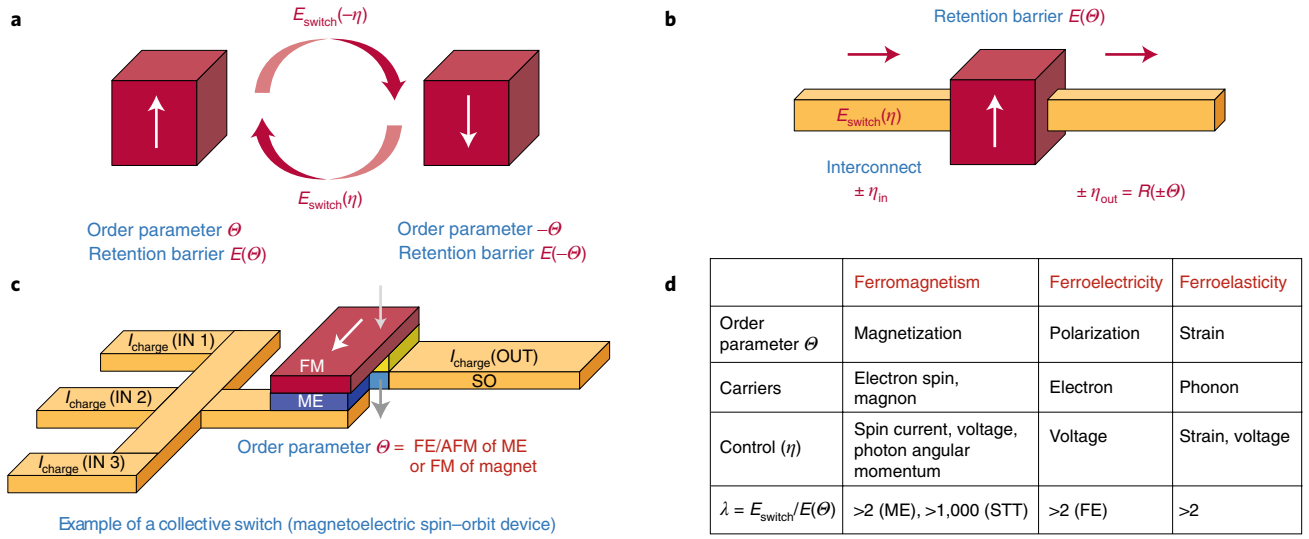

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	Ferromagnetism	Ferroelectricity	Ferroelasticity
Order parameter Θ	Magnetization	Polarization	Strain
Carriers	Electron spin, magnon	Electron	Phonon
Control (η)	Spin current, voltage, photon angular momentum	Voltage	Strain, voltage
$\lambda = E_{switch}/E(\Theta)$	>2 (ME), >1,000 (STT)	>2 (FE)	>2

Fig. 1 | Definition of a collective switch. a, Collective state switch for using the materials' order parameter. The two states are given by values of $\pm\Theta$. **b**, Interconnect providing an input to and output from the switch carries a signal $\pm\eta$. The state of the device is detected and transduced to the output $\pm\eta_{out} = R(\pm\Theta)$. **c**, Example of a collective switch, a magnetoelectric spin–orbit logic device[13] where the order parameters are ferroelectric/antiferromagnetic (FE/AFM) of the magnetoelectric (ME), and the read-out is via spin–charge conversion. **d**, Potential order parameters, carriers and control variables are shown. The figure of merit $\lambda = E_{sw}/\Delta E(\Theta)$ allows identification of potential for an efficient logic device/switch. STT, spin-transfer torque.

Table 1 | Materials targets for computing with spin and polarization for beyond-CMOS devices

Target	Device/material figure of merit	Challenge target (T > 420 K)	Example of state of the art
Magnetic/FE/MF switching (10 × 10 nm^2)	Switching energy	1–10 aJ	20 aJ (all optical); for example, ref. [41]
			400 fJ per bit; for example, ref. [42]
	Switching voltage	100–300 mV	100 kV cm^{-1} $LaBiFeO_3$ (ref. [43])
			250–400 mV perpendicular spin transfer torque (STT)[44,45]
	Switching speed	10–1,000 ps	120 ps (nominal)[42], <3 ns (STT)[45]
	Write error rate	10^{-1} (stochastic)[46,47]–10^{-12} (von Neumann)	10^{-10} (STT)[45], 10^{-5} (ME)[56]
	ME/FE	P_c ~ 0.5–5 μC cm^{-2}	Refs [43,47]
		Converse magnetoelectric coefficient $\Delta H/\Delta V$ ~ 10 C^{-1}	$BiFeO_3$ (refs [22–26]), $BiFeO_3/CoFe_2O_4$, Terfenol-D/PZT; for example, ref. [48]
	Spin–orbit coupling (SOC) switching	λ_{IREE} (for switching) > 10 nm, ρ_{soc} < 10 μΩ cm	Refs [49,51,52,66]
		Δ/I_c >10	For example, ref. [53]
Spin detection (10 × 10 nm^2)	Spin to charge efficiency	I_c/I_s > 90–100%	For example, refs [54,55]
	Read-out voltage	>100 mV	For example, ref. [54]
	SOC detection	λ_{IREE} (for read-out) >10 nm, ρ_{soc} > 10 mΩ cm	Refs [49,51,52,66]
Interconnect	Switching voltage, currents	100 mV, 1–10 μA	
	Dimensions — local interconnect	30-nm width, 100 nm–0.1-mm range	For example, ref. [2]
	Spin-optical/vice versa conversion	< 10 aJ per bit, 1 Gbit s^{-1}	For example, ref. [41,67]
	Dimensions for optical	200-nm width, >100-μm range	Ref. [57]
Nanomagnet/FE/MF	Stability (Δ/k_BT)	40 (logic)–80 (memory)	For example, ref. [44]
	Spin injection	>80 %	For example, Heusler alloys[58]

energy $E(\Theta)$ on the order parameter Θ. The value of the energy barrier is related to the device's retention time and determines the non-volatile nature of the switch. The logic state is retained in the order parameter (Θ) and the output logic signal is generated via an efficient read-out (through transduction of the state to a communication/interconnect state variable) mechanism, where the read

signal is $R(\Theta)=-R(-\Theta)$. For example, for magnetoelectric spin–orbit logic (Fig. 1c) based on magnetoelectric switching of a multiferroic[13], Θ is the order parameter of the multiferroic (coupled polarization **P** and antiferromagnetic order L) and η is the charge voltage on the interconnect. For spin torque logic with spin interconnects[21], Θ is magnetization **M** and η is the spin current I_s. For a magnon transistor[12] Θ is magnetization and η is the phase of magnons on the interconnect.

We define a figure of merit for collective switches as:

$$\lambda = E_{sw}/\Delta E\,(\Theta)$$

where $\Delta E(\Theta)$ is the energy barrier relative to the stable order parameter, and E_{sw} is the total energy dissipated in switching. Lower values of λ enable computing switches to operate at lower energy for a given energy barrier. The energy barrier $\Delta E(\Theta)$ of a collective switch is set by the technology requirements. For example, a logic circuit may need to preserve the state of the switch long enough for computation. The factor λ is the figure of merit due to the following reasons: (a) for a given type of logic operation, $E(\Theta)$ is set by the stability of the logic state needed — the derivation of the $E(\Theta)$ requirement follows the arguments of Landauer, and is discussed later; (b) $E_{sw}/E(\Theta)$ provides the efficiency of switching, normalized for state retention; and (c) the ratio relates $E(\Theta)$, a parameter of the materials stability given by the order (magnetism/polarization/strain), with the switching energy, which comprehends the losses and dynamics of switching.

Lower bounds to λ under technology constraints provide an insight into the choice of beyond-CMOS devices (Table 1). The factor λ is >2 for capacitive, magnetoelectric and ferroelectric devices, and it can be as high as 10^4 for spin torque devices. Let us contrast the switching of a device with spin torque and ferroelectric/magnetoelectric effects. The inefficiency of switching a magnet with spin currents and magnons (spin waves) can be an intrinsic limitation. When we compare the energy stability, a single Bohr magneton contributes $E_{M_B B} = (1/2)\mu_B B_k \sim 0.1$–1 meV at an equivalent magnetic anisotropy of B_k 0.1–1 T). In contrast, electric charge of a single electron contributes to large electrostatic energy ($E_{Ee} = eV_c \sim 100$–1,000 meV at V_c 0.1–1 V). This directly contributes to the disparity in the number of carriers needed for switching and the figure of merit λ. Due to the small magnetic stability of a single Bohr magneton, the number of electron spins required to form an energy barrier of 1 eV is $\sim 2\Delta E(\Theta)/\mu_B B_k \sim$ 1,000–10,000, requiring injection of 1,000–10,000 spins for magnetization reversal. In contrast, the number of electrons required to form an electrostatic energy barrier of 1 eV is $\Delta E(\Theta)/eV_c \sim 1$–10, allowing for very efficient polarization/magnetization reversal. Furthermore, the Joule energy losses due to large spin currents further increase the inefficiency of switching with spin torque.

This fundamentally indicates that a switch with polarization (electric dipole) as the primary order parameter provides an intrinsically better path to energy efficient switches. Magnetoelectric mechanisms[22–24], especially in multiferroic materials, allow the use of ferroelectricity as the dominant order parameter providing a potential for extreme energy efficiency[25–28].

Interconnects from a thermodynamic perspective

The interconnect carries a signal parameter η, such as charge, spin number or helicity of photons, which can induce a change of state in the switch. Figure 1b shows the interconnect as a physical connection between two switches. Interconnects should carry the state of the prior logic stage via amplitude/phase/angular momentum of the carriers and trigger a switching event (reversal of Θ) at the receiving logic stage switch. The read-out mechanism from the switch provides a sign-dependent read-out of the interconnect state — the readout mechanism must have odd symmetry in order to carry the information of the state of the switch.

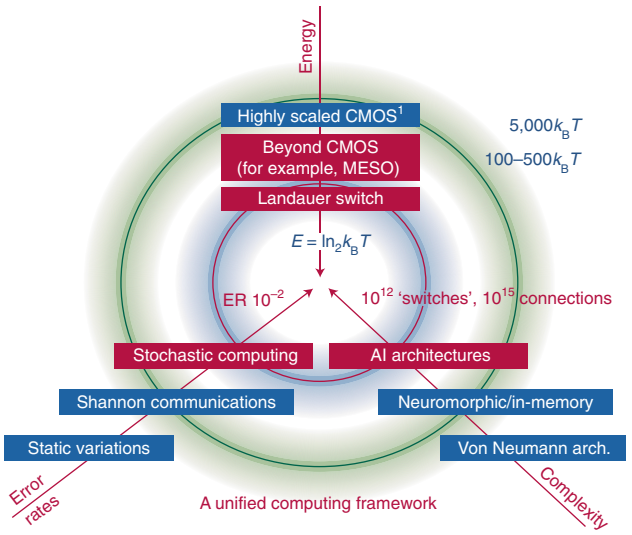

Fig. 2 | A unified computing framework comprising three axes for scaling. Top: energy scaling axis, representing the reduction in switching energy per device. Bottom-left: error rate scaling axis, representing the ability to function/compute with higher error rates. Bottom-right: complexity scaling axis, representing the ability to productively utilize an increased number of devices in scalable architectures.

We next consider interconnects from the perspective of detector thermodynamics and show the potential for extremely low-voltage (<100 mV) nanoelectronic interconnects, working with a potentially low-voltage beyond-CMOS device. The fundamental limit to the operating voltage of an electrical interconnect, assuming a switch is also able to operate at the given low voltage, is given by the Shannon–Nyquist relationship between noise voltage v_n and the receiver capacitance C: $\sqrt{\delta v_n^2} = \sqrt{k_B T/C}$, where k_B is the Boltzmann constant and T is temperature. It can be expressed as variation of number of electrons n_n as $\sqrt{\delta n_n^2} = \sqrt{k_B TC}/e$. At a capacitance of 10 aF, the noise voltage is 20 mV and the charge noise is 1.27e. For example, a 100-mV charge interconnect driving a ferroelectric/multiferroic capacitor with a charge density $P_c = 10$ μC cm^{-2} operating at 100 nm^2 of device area can operate above the electronic Shannon–Nyquist noise limits. In addition, it is critical to lower the electrical current of the interconnect along with the operating voltage swing to compensate for the rise in electrical resistivity at reduced dimensions (W) (ref. [29]) where the dimension of the wire (W) is comparable to the electrical mean free path of the carriers.

We next consider interconnects from intrinsic insertion losses (loss of signal strength per unit length) and size scalability, and note a fundamental shortcoming of the spin current/diffusion interconnects. For spin interconnects the carriers are spin currents, which are not conserved ($\nabla s \neq \mathbf{J}_s$) due to spin scattering. Practically, this leads to insertion losses of the spin currents exceeding 4.3 dB μm^{-1} at 1-μm channel widths, assuming spin diffusion lengths of 1 μm. Practical interconnects used in integrated circuits have already been scaled to sub-100 nm, with the densest interconnects ~30 nm in width to match to the size-scaled transistors[1]. This implies that all new interconnect technologies must be considered at scaled width sizes. It is a commonly held notion that pure spin interconnects could be energy efficient due to dissipationless propagation of the spin currents. However, for practical computational logic circuits, the need for regeneration — spin signal repeaters or regenerators, which comprise a switch — to compensate for spin-scattering insertion losses imposes a high penalty for spin interconnects[30,31].

In contrast to their spin counterparts, electronic interconnects provide long-range signal propagation (exceeding hundreds of

Box 1 | Milestones and challenges for spintronic logic

We describe the grand scientific and technological challenges for implementing spintronic logic devices. We divide these challenges into three classes: magnet/spin switching, magnet/spin detection and interconnect and complexity challenges. We also provide a list of figures of merit (Table 1) that will accelerate the introduction of the spintronic integrated circuits.

Problems of magnetic/multiferroic switching.

1. How to switch a magnetic/multiferroic (MF) state in volume of 1,000 nm^3 with a stability of $100k_BT$ and an energy of 1 aJ ~ 6.25 eV ~ $240k_BT$?
2. What are the timescales involved with magnetoelectric/ferroelectric (FE)[59]/MF[60] switching of a magnet/FE/MF at scaled sizes? How to overcome the Larmor precession timescale of a ferromagnet[61]?
3. How to switch a scaled magnet/polarization switch with low stochastic errors[62]? What are the fundamental mechanisms governing the switching errors, fatigue for scaled FE/ME switching[63]?
4. What is the right combination of materials/order parameters for practical magnetoelectric switching (for example, multiferroic FE/antiferromagnet (AFM) plus FM[2223–26], paraelectric/AFM plus FM[27], piezoelectric plus magnetostriction[64])?

Problems of magnetic state detection. MgO-based tunnel junctions[10] have enabled a practical solution to the detection of a magnetic state in solid-state devices. However, low tunnelling magnetoresistance, high impedance, which requires ultrathin MgO to meet practical constraints, and high voltage (due to tunnelling) limit the long-term potential for spintronic integration. Hence, fundamentally new read-out mechanisms not reliant on MgO tunnel barriers, such as giant magnetoresistance, non-tunnelling metallic/semimetallic read-out and spin to charge conversion methods, are a technology priority.

5. How to detect the state of a magnet/ferroelectric with high read-out voltage >100 mV? For inverse spin–orbit effects, such as the spin galvanic effect/Edelstein effect[65,66], how to achieve $\lambda_{IREE} > 10$ nm with high resistivity[49,53]?
6. What is the scaling dependence of spin–orbit detection of the state of a magnet? How to detect the state of a perpendicular magnet with spin–orbit effect?

Problems of interconnects and complexity.

7. How to transfer the state of a magnet/FE over long distances on scaled wire sizes (<30-nm-wide wires with pitch <60 nm)? In particular, how to improve the spin diffusion interconnects in non-magnetic conductors and magnon interconnects in magnetic interconnects?
8. How to transduce a spintronic/multiferroic state to a photonic state (and vice versa) to enable very long distance interconnects (>100 μm)[67]?
9. The back-end of CMOS comprises multiple layers of metal wires separated by a dielectric. Thus making logic devices between these layers requires starting with an amorphous layer and a template for growth of the functional materials. How to integrate the magnetic/FE/MF materials in the back-end of the CMOS chip[50,68]?
10. How to utilize stochastic switches (spin/FE) operating near practical thermodynamic conditions in a computing architecture[17,18,69]?
11. How to utilize the extreme scaling (with size, logic efficiency and three-dimensional integration) feasible with spin/FE devices in a computer architecture in order to achieve 10 billion switches per chip[18,19]?

micrometres)[32] owing to the charge conservation ($\nabla Q = \mathbf{J}_c$). The insertion losses at scaled sizes for electrical interconnects is close to zero, limited by dynamic resistor–capacitor leakage currents. Hence, from an insertion-loss and size-scalability perspective, electrical interconnects continue to be the most suitable for short-distance, highly scaled interconnects. For longer range interconnects, with >100 μm length and >200 nm width, for high bandwidth density (>100 Gbit s^{-1} μm^{-1}), nanophotonic interconnects come into play[32].

Limit to computing energy per device at practical switching

The intrinsic limit to computing energy per device at practical switching speeds (few GHz) and retention times (few seconds) calculated below are ~$100k_BT$, which is a factor of ~50 smaller than for the aggressively scaled CMOS. This suggests that it is possible for computational devices to be created that would enable orders of magnitude improvements in computational scaling. The Landauer limit for energy dissipation is $k_BT\ln(2)$ for irreversible logic operations. This limit holds asymptotically as the delay of the logic operation goes to infinity[33]. For finite switching-time operation and finite switching error rate requirements, the minimal retention barrier $\Delta E(\Theta)$ and minimal switching energy E_{sw}, as a function of the retention error probability ϵ, a finite switching time T_s and the characteristic time of thermal fluctuations T_{therm} are given as follows:

$$\Delta E(\Theta) > k_B T\left[\ln\left(\frac{1}{\epsilon}\right) + \ln\left(\frac{T_s}{T_{therm}}\right)\right]$$

$$E_{sw,min} > \lambda k_B T\left[\ln\left(\frac{1}{\epsilon}\right) + \ln\left(\frac{T_s}{T_{therm}}\right)\right]$$

As noted by Landauer, accounting for switching errors due to finite switching speeds and for retention error due to a finite barrier leads to this correction[33,70]. For $\epsilon = 10^{-15}$, $T_s/T_{therm} = 10^9$ and $\lambda = 2$, $E_{sw,min} \sim 110\ k_BT$. Please see Box 1 where we propose a technological milestone for a switch operating at 250 k_BT or 1 aJ . Note that computing methods tolerant to stochasticity, due to retention errors or finite switching time, will allow for further reductions in the computing energy per bit, as discussed in the unified computing framework (Fig. 2).

A unified computing framework

We finally describe a unified computing framework to represent computing evolution along three distinct dimensions: energy per switching device, device switching error rate and architectural complexity of the computational unit (excluding the memory) (Fig. 2). These three axes represent the beneficial scaling enabled by novel physics, materials and devices (energy/switch axis), application of information theory/error resilience techniques (device switching error rate), and architectural innovations allowing for larger number of devices to be utilized in a productive manner (complexity/computational unit).

Traditional scaling of transistors, enabled by size scaling, new structures and materials, have propelled energy per device and

complexity scaling. On the energy axis, gains in switching efficiency due to a reduction in the device size and applied voltages led to the highly scaled CMOS transistor operating at ~$10^4 k_B T$. The future device options enabled by spintronics/ferroelectrics have a possibility to scale the device switching energy to $100 k_B T$, provided the milestones (Box 1) for logic technology can be surpassed.

The ability to productively utilize larger numbers of switches enabled by energy and size scaling is represented on the complexity axis. The number of transistors per CPU has increased, keeping in sync with the increasing transistor density (10–50 million transistors per CPU), but ultimately being limited by the scalability of traditional von Neumann architectures[3]. However, recent architectural innovation in neuromorphic/in-memory/artificial intelligence represent a new opportunity for allowing higher complexity architectures that take advantage of the high transistor density allowed by modern CMOS processes.

Traditional von Neumann/Turing architectures[3], neuromorphic architectures[20,34], collective processors, such as networks of nano-oscillators[35], and emerging artificial intelligence architectures[35–38] are positioned on the axis of complexity scaling. Complexity theory provides great insights into the collective behaviour of macroscopic (mesoscale) objects, including the ability to provide computation via emergent behaviours[39,40]. Historically, the complexity of electronic computer architectures has stagnated near 10–100 million transistors per core due to design trade-offs between computing dynamic power and leakage power, operating voltage versus clock speed, and the optimum instructions per clock — and increasing transistor density has been applied to increase the size of the on-chip memory and additional functionality. Advances in neuromorphic/cognitive computing and emergent behaviour of collective systems can play an important role (Box 1, grand challenge 11).

In sharp contrast to energy per bit and complexity per CPU, the computational switching error rates have been kept extremely low ($<10^{-14}$) via classical computer/circuit design techniques. Exceptions utilizing high error rates have been limited to data interconnects operating over long distances or large memory banks. Error rates in communication, computation and memory arise from intrinsic/extrinsic noise sources, static variations and the choice of digitization (quantization) representation. In present digital computation, the physical digital logic layers operate at nearly error-free regimes (logic error rate $< 10^{-14}$) since modern computing is built under the assumption of nearly error-free dynamic operation. Process variations (lithographic imperfections, dopant fluctuations) are overcome by strong overdesign of the circuits.

In the field of communications, the great success of Shannon's information theory has enabled communications at length scales from 10^6 km to 10 m, providing a tool set based on the model of a noisy channel. We posit that Shannon's approach[18,69] can be extended to computing (logic and memory) starting with a well described theory for the stochasticity for scaled devices. We propose that new architectures and methods be developed to allow computing fabrics to be erroneous. Advances on the computational theory in approximate and stochastic computing can play an important role (Box 1, grand challenge 10). The recent development of approximate computing processors with reduced and variable precession also lie on this axis, where the systematic quantization/digitization error may be increased due to the nature of the computational work (for example, inference or recognition tasks)[37,38].

Scaling along all the three axes will lead to a unified computing paradigm that needs to switch at $100 k_B T$ per event, tolerate high switching error rates, due to intrinsic/extrinsic stochasticity and thermodynamic constraints, and be able to utilize >10 billion switches operating in a collective/cooperative way.

In conclusion, a distinct opportunity and direction to continue Moore's law scaling via new materials, devices and state variables exists. Spintronics and multiferroics are the leading candidates owing to the potential for ultralow switching energy (1 aJ per switch) at ultralow switching voltages (<100 mV). However, this requires great advances in experimental and theoretical understanding of the materials, devices and circuits. We provide a list of grand challenge milestones, which systematically address the key performance metrics. We also describe a unified computing framework, which maps scaling along energy, switching error rates and complexity.

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Competing interests

The authors declare no competing interests.

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