In-Memory Processing Paradigm for Bitwise Logic Operations in STT-MRAM

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In current big data era, the memory wall issue between the processor and the memory becomes one of the most critical bottlenecks for conventional Von-Newman computer architecture. In-memory processing (IMP) or near-memory processing (NMP) paradigms have been proposed to address this problem by adding a small amount of processing units inside/near the memory. Unfortunately, although have been intensively studied, prior IMP/NMP platforms are practically unsuccessful because of the fabrication complexity and cost efficiency by integrating the processing units and memory on the same chip. Recently, emerging nonvolatile memories provide new possibility for efficiently implementing the IMP/NMP paradigm. In this work, we propose a cost-efficient IMP/NMP solution in STT-MRAM without adding any processing units on the memory chip. The key idea behind the proposed IMP/NMP solution is to exploit the peripheral circuitry already existing inside memory (or with minimal changes) to perform bitwise logic operations. Such an IMP/NMP platform enables rather fast logic operations as the logic results can be obtained immediately through just a memory-like readout operation. Memory READ and logics NOT, AND/NAND, OR/NOR operations can be achieved and dynamically configured within the same STT-MRAM chip. Functionality and performance are evaluated with hybrid simulations under the 40 nm technology node.

***Index Terms*—STT-MRAM, in-memory processing (IMP), near-memory processing (NMP), nonvolatile memory.**

I. Introduction

In current big data era, the limited data bandwidth between the processor and the memory has become one of the most critical bottlenecks for conventional Von-Newman computer architectures. At the same time, the data transfer between the processor and the memory consumes high latency and energy, significantly degrading the system performance and efficiency. These issues are known as "memory wall" and "power wall", posing unprecedented challenges for computing capability to handle the ever-growing big data [1, 2]. In-memory processing or near-memory processing (IMP/NMP) paradigm, a decades-old concept, has been proposed to address this problem by adding a small amount of processing units inside/near the memory [3, 4]. The basic idea behind is that instead of moving all the raw data to the processor, it pre-processes the raw data and provides the processor only the intermediate results. Such a paradigm can reduce the overhead of data transfer bandwidth and power as well as improve performance by performing simple yet bandwidth-intensive logic operations in/near the memory. Unfortunately, although have been intensively studied, prior IMP/NMP platforms are practically unsuccessful, because manufacturing the performance-optimized processing units and the density-optimized memory on the same chip/die is rather complex and is not cost-effective.

Recently, emerging nonvolatile memories [5-7], such as resistive random access memory (ReRAM), phase change memory (PCM) and spin-transfer torque magnetic random access memory (STT-MRAM) etc., provide new possibility for efficiently implementing the IMP/NMP paradigm [3, 8-11]. On one hand, the 3D-stacking functionality of the nonvolatile memory devices enables to decouple the logic and memory circuits in different manufacturing processes with the back-end-of-line (BEOL) process technology, significantly alleviating the fabrication complexity and cost [12]. On the other hand, the resistance-based storage mechanism of the nonvolatile memory devices provides inherent processing capability, thus enabling energy-efficient logic computing within the memory. In this case, logic operations can be performed and the results are stored in the memory chip nonvolatilely. Therefore, IMP/NMP has recently reignited interest among industry and academic communities driven by the recent advances in these nonvolatile memory technologies [3, 13-18]. For example, "Pinatubo" in [3] has been designed for bulk bitwise logic operations in emerging nonvolatile memories, which, however, may not be employed directly for STT-MRAM owing to the low TMR ratio. Thereby, different strategies should be exploited for different nonvolatile memories, considering their intrinsic properties.

In this work, we propose a cost-efficient IMP/NMP solution for STT-MRAM having complementary array structure without adding any processing units on the memory chip. The key idea behind the proposed IMP/NMP solution is to exploit the peripheral circuitry (e.g., the sensing amplifier) already existing inside memory (or with minimal changes) to perform bitwise logic operations. Such an IMP/NMP platform enables fast and reliable logic operations as the logic results can be obtained immediately through just a memory-like readout operation. With the proposed IMP/NMP platform, memory READ and logic NOT, AND/NAND, OR/NOR operations can be achieved and dynamically configured within the same STT-MRAM chip.

The remainder of this paper is organized as follows. Section II briefly introduces the fundamentals of STT-MRAM. In Section III, we present the IMP/NMP paradigm in STT-MRAM. Section IV illustrates our simulation and discussion. Finally Section V concludes this paper.

Manuscript received March 10, 2017; Revised April 7, 2017.
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Digital Object Identifier (inserted by IEEE).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TMAG.2017.2703863, IEEE Transactions on Magnetics

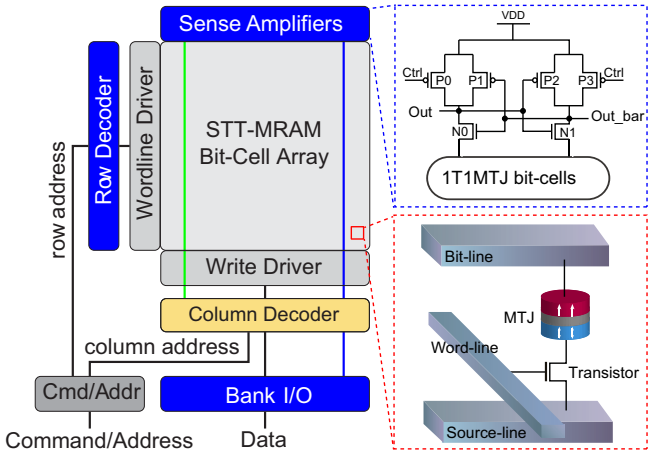

Fig. 1. Schematic of a STT-MRAM bank and the associated 1T1MTJ bit-cell structure and sensing amplifier.

II. STT-MRAM FUNDAMENTALS

Fig. 1 shows the schematic of a STT-MRAM bank and the associated 1T1MTJ (i.e., one Transistor connected in series with one Magnetic Tunnel Junction) bit-cell structure and the peripheral sensing amplifier. The MTJ device is used as storage element while the transistor acts as an access device. An MTJ is mainly composed of three ultra-thin layers: one oxide barrier layer (e.g., MgO) sandwiched between two ferromagnetic (FM) layers (e.g., CoFeB). An MTJ can present two resistance states (i.e., low resistance, R_P and high resistance, R_{AP}) depending on the relative magnetization orientation (parallel (P) or anti-parallel (AP)) of the two FM layers. The resistance difference between the two stable resistance states of the MTJ device is characterized by the tunnel magneto-resistance (TMR) ratio (TMR $= (R_{AP} - R_P)/R_P$). The STT-MRAM memory bank is organized with an array of 1T1MTJ bit-cells through multiple bit-lines (BLs), word-lines (WLs), source-lines (SLs) and peripheral circuits, such as row/column decoders, write/read drivers as well as input/output (I/O) interfaces. To write data bit into the bit-cell, only a bi-directional current (through the STT mechanism [19]) is required through the write driver to change the magnetization orientation of the free layer of the MTJ. Due to the TMR effect, the digital information stored in the MTJ device of the bit-cell can be readout by distinguishing the resistance of the MTJ device in the memory bit-cell from that of a reference cell, in which the resistance of the MTJ is pre-known and is generally set to $(R_{AP} + R_P)/2$ [20, 21]. Here we consider a complementary memory cell array in STT-MRAM considering the limited TMR ratio (which is generally below 200% at room temperature) of the MTJ devices [8]. In such a configuration, we require no reference cell and the digital information stored in the memory is readout by comparing the resistance difference between the two complementary bit-cells (through BLs) via sensing amplifiers (SAs). Here we choose the pre-charge sensing amplifier (PCSA) in our design [22], as it provides fast sensing speed, high reliability and low power consumption. The read operation of the PCSA can be divided into two stages depending on the control signal and is described as follows. During the pre-charge (reset) phase (WL = 0 V and Ctrl = 0 V), the four PMOS transistors P0-P3 turn on and they charge the nodes "Out" and "Out_bar" to V_{dd}. During the discharging and evaluation stages (WL = V_{dd} and Ctrl = V_{dd}), nodes "Out" and "Out_bar" begins to discharge but with a different rate owing to the different resistances between the two complementary bit-cells (Bls). Then a differential voltage ΔV will build up between the two BLs (also between nodes "Out" and "Out_bar"). Once either "Out+" or "Out-" becomes less than the switching threshold voltage of the transistor in the cross-coupled inverters, composed of P1-P2 and N0-N1, they begin to amplify the voltage difference between "Out+" and "Out-" nodes, then either "Out-" or "Out+" node will be charged to V_{dd} or '1', while the other one will continue discharging to Gnd or '0'. Therefore the data stored in the bit-cells will be readout. Note that there are never any stationary currents during the sensing operation, only dynamic charging or discharging currents, we can expect very high speed and low power consumption. The details on the implementation and operation of the other peripheral circuits are not the focus of this paper and thus are omitted here.

III. PROPOSED IMP/NMP PARADIGM IN STT-MRAM

As discussed in the previous section, the data read operation in STT-MRAM is to compare the resistances of the MTJs in the two complementary bit-cells along the BLs through a SA. Since multiple WLs share the same set of SAs or BLs, the final output state of the SA depends solely on the resistances of the BLs connected to the two branches of the SA. In this configuration, we can perform bitwise logic operations by activating two (or more) WLs simultaneously, as shown in Fig. 2(a), which is an example of a 2-input AND or OR operation (see the truth table in Fig. 2(b)). Here the data stored in WL1 and WL2 are the two operands, while the data stored in WL0 are the control operands determining the logic types (either AND or OR). Specifically, if the data in WL0 are 1s, then the outputs of the SAs are bitwise OR of the data in WL1 and WL2. Otherwise, if the data in WL0 are 0s, then the outputs of the SAs are bitwise AND of the data in WL1 and WL2. Fig. 3 shows the detailed schematic combing the PCSA circuit. The data stored in the bit-cells along WL0 can be variable in order to perform different logic operations (either AND or OR) for different BLs. Furthermore, by adding an inverter (INV) and a multiplexer after the each SA, bitwise memory READ/NOT, NAND/NOR operations can then be achieved. Because of the regular bulk operation of bit-cells along the WLs in STT-MRAM, this approach naturally enables bulk bitwise READ/NOT, AND/OR and NAND/NOR logic operations through the SAs. Moreover, such an IMP/NMP platform enables rather fast logic operations as the results can be obtained immediately through just a memory-like readout operation. In addition, the processing is nondestructive and the logic operands and results can be statefully stored locally in the memory owing to the nonvolatility of the STT-MRAM bit-cells.

As can be seen, by modifying the row decoder and the SA, bitwise READ/NOT, AND/NAND, OR/NOR operations can be achieved with very little hardware overhead via our proposed

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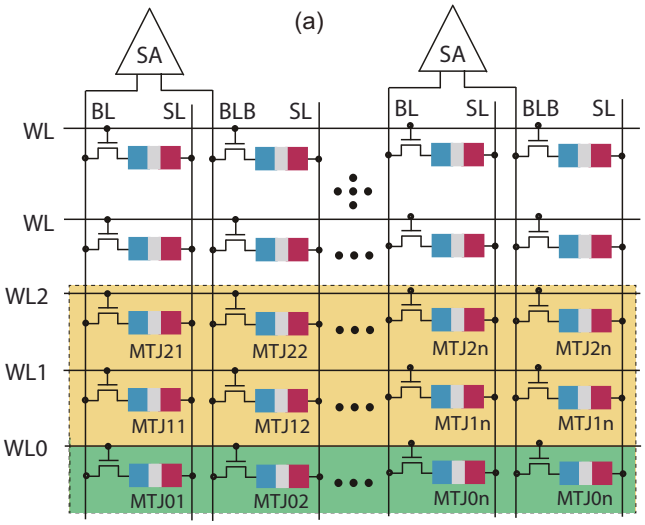

(b) Turth table for the AND and OR operations

Logic gate	Data in WL0 (MTJ 01, 02)	Data in WL1 (MTJ 11, 12)	Data in WL2 (MTJ 21, 22)	Output of the SA
AND	0 (P, AP)	0 (P, AP)	0 (P, AP)	0
	0 (P, AP)	0 (P, AP)	1 (AP, P)	0
	0 (P, AP)	1 (AP, P)	0 (P, AP)	0
	0 (P, AP)	1 (AP, P)	1 (AP, P)	1
OR	1 (AP, P)	0 (P, AP)	0 (P, AP)	0
	1 (AP, P)	0 (P, AP)	1 (AP, P)	1
	1 (AP, P)	1 (AP, P)	0 (P, AP)	1
	1 (AP, P)	1 (AP, P)	1 (AP, P)	1

Fig. 2. Illustration of (a) the proposed IMP/NMP paradigm for bitwise AND/OR operations in STT-MRAM, and (b) the corresponding truth table.

IMP/NMP paradigm within a STT-MRAM. The data stored in the STT-MRAM can be straightforwardly readout or processed by dynamically configuring the peripheral circuits depending on practical requirements. It should be noted that for data stored in the same STT-MRAM bank, the bitwise logic operations are rather simple. For data stored in different memory banks or sub-arrays, data movements within the memory chip are required to implement the logic operations, which, however, do not occupy the bandwidth between the processor and memory. In addition, system/software supports are generally required to implement the IMP/NMP paradigm, which are beyond the scope of this paper. More details about the system/software supports can refer to [3]. The proposed cost-effective IMP/NMP platform is very useful for some specific applications (e.g., bitmap) that rely on bulk bitwise logic operations on large bit-vectors.

IV. Evaluation and Discussion

By using a commercial CMOS 40 nm design kit and an in-house developed perpendicular anisotropy CoFeB/MgO STT-MTJ compact model [23], hybrid STT-MTJ/CMOS simulations are performed to demonstrate the functionality and performance of the proposed IMP/NMP platform in STT-MRAM. Here the

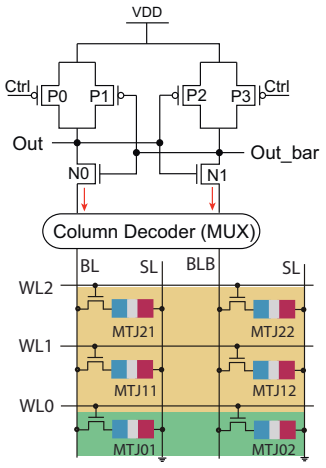

Fig. 3. Proposed IMP/NMP paradigm for bitwise 2-input AND/OR operations with the PSCA circuit.

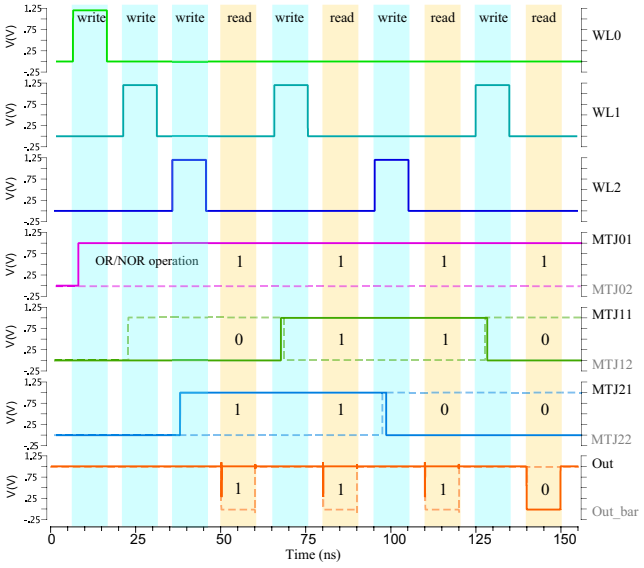

Fig. 4. Transient waveforms of the OR/NOR operations with the proposed IMP/NMP platform in STT-MRAM.

supply voltage is $V_{dd} = 1.2\,\mathrm{V}$, and the TMR = 100%. We use the minimum feature size for all the CMOS transistors and the default values for the STT-MTJ model can refer to [23].

Fig. 4 and Fig. 5 show the transient simulation waveforms of the OR/NOR and AND/NAND operations with the proposed IMP/NMP platform respectively. Initially, we activate each WL to write the initial data into the bit-cells. Then we change the data along the WLs to verify the functionality of the logic operations. As can be seen, the latency (~200 ps) for performing logic operations is similar to that of reading a data bit from the memory bit-cells. Further, we can also configure the data stored in the bit-cells along WL0 to dynamically configure the logic types for different BLs. The transient simulations validate the correctness of the proposed IMP/NMP design in STT-MRAM. It should be noted that as the bit-cells along the WLs are parallel connected during the logic operation mode, the real resistance difference between the two BLs will be degraded compared to that of the memory mode. In this case, the sensing reliability of

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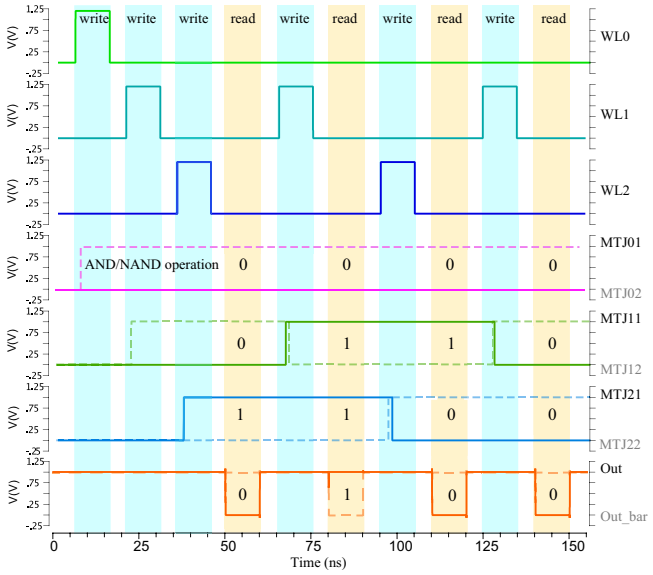

Fig. 5. Transient waveforms of the AND/NAND operations with the proposed IMP/NMP platform in STT-MRAM.

the SA will be affected because of reduced real TMR ratio and increased parasitic parameters. Therefore, higher TMR ratio of the MTJ devices and sensitive SAs (e.g., separated PCSA [24] and tunneling negative differential resistance-assisted SA [25]) are preferred in the proposed IMP/NMP platform.

V. Conclusion

A cost-efficient IMP/NMP platform is proposed here in STT-MRAM for bitwise logic operations to address the memory wall and power wall issues. Without adding any processing units, the proposed IMP/NMP platform performs logic operations within the memory through exploiting the peripheral circuitry already existing inside memory. Memory READ/NOT, AND/NAND, OR/NOR operations can be achieved within the STT-MRAM chip. Our simulations demonstrate that the proposed IMP/NMP platform enables rather fast logic operations as the logic results can be obtained via just a memory-like readout operation. More efforts on system or software hierarchy are expected to support the proposed IMP/NMP paradigm.

Acknowledgment

This work was supported by the National Natural Science Foundation of China (Grant 61501013 and 61571023).

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