Fully integrated 54nm STT-RAM with the smallest bit cell dimension for high density memory application

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Abstract

A compact STT(Spin-Transfer Torque)-RAM with a $14F^2$ cell was integrated using modified DRAM processes at the 54nm technology node. The basic switching performance (R-H and R-V) of the MTJs and current drivability of the access transistors were characterized at the single bit cell level. Through the direct access capability and normal chip operation in our STT-RAM test blocks, the switching behavior of bit cell arrays was also analyzed statistically. From this data and from the scaling trend of STT-RAM, we estimate that the unit cell dimension below 30nm can be smaller than $8F^2$.

Introduction

As conventional memories (DRAM, NAND) scale down towards the technology limit, it is becoming increasingly important to find suitable alternatives. STT-RAM (Spin-Transfer Torque-RAM) has unlimited endurance, the highest reliability of any non-volatile memory, and fast random access capability, so it could be a promising candidate. In addition, the STT write operation gives better scalability than conventional switching by magnetic field. However, in order to be competitive with existing low cost memories, it is necessary to make a DRAM comparable unit cell dimension while maintaining bit cell performance such as cell current drivability and MTJ (magnetic tunnel junction) thermal stability. The unit cell dimensions reported by other groups are typically larger than $40F^2$ [1,2], because the access transistors were made with conventional logic processes. In this work, we used a very compact DRAM process to minimize the cell dimension and evaluated the performance of memory bit cells in a highly integrated STT-RAM. We forecast that STT-RAM will be a promising candidate for future memory.

Process Integration of STT-RAM

To achieve sufficient operation margin in non-volatile memories, it is necessary to increase the current drivability and to reduce the resistances of line, plug, and contact in the limited area. We therefore carefully designed the cell array architecture and its process. Figure 1 shows the MTJ top view image, the TEM cross section image for a compact cell array and the key process for our STT-RAM. The cell transistor structure is not much different from conventional DRAM which uses a self-aligned contact and plug process. The only major differences are the introduction of a source line SL (parallel to bit line BL), metal plug and FinFET cell transistor. We used low resistive W for the SL and BL. We also placed the MTJ directly above the bottom electrode (BE) contact to maximize the cell packing density.

We used in-plane MTJs rather than PMA (perpendicular magnetic anisotropy) MTJs [3]. Although many research groups have tried to develop productive PMA MTJs, the PMA MTJ still has several technical hurdles such as difficult PMA film growth and high damping constant [4]. Also, we do not yet have confidence that PMA MTJs can have better scalability than in-plane MTJs in terms of thermal stability and switching current [5]. Our MTJs have an advanced in-plane structure that includes top electrode / partial perpendicular magnetic anisotropy (PPMA) capping layer / CoFeB based free layer / MgO tunnel barrier / synthetic pinned layer / anti-ferromagnetic PtMn / seed Ta. The switching current density of our MTJs is reduced due to the PPMA capping layer and free layer engineering [6,7]. The MTJ dimension is ~54x108nm near the MgO layer. We successfully developed an MTJ RIE process that suppresses shunting and edge damage. In this work, we did not use additional MTJ connection processes such as extended bottom electrode (connecting the MTJ and bottom plug) and top electrode plug between MTJ and M1. Since the MTJ is directly connected to the bottom plug and to M1, we could provide a more simplified MTJ module process and smaller unit cell dimension compared to any other reports.

Figure 2 shows the cell array layout and schematic for memory cell operation. In this work, we were able to achieve the required current drivability of the cell transistor using dual access cell transistors with wider active width than conventional DRAM cell transistors. The unit cell dimension used was $14F^2$ (WLxBL=3.5F×4F) at the 54nm technology node.

Memory bit cell characteristics

In a unit bit cell with cell transistor and MTJ, the current drivability of the cell transistor depends on the MTJ resistance states, the parasitic resistance and the write / read operation bias conditions. In particular, the cell transistor shows different performance for write 1 (parallel to anti-parallel switching) and write 0 (anti-parallel to parallel switching) [8]. Figure 3 shows that the current drivability of the cell transistor for write 1 operation is lower than that for write 0 operation, because the voltage across the MTJ lowers V_{GS} of the cell transistor during write 1 operation. In our system, the write 1 current drivability of the cell transistor is ~140uA.

The RIE process is a critical element of the pattering process for densely-packed MTJ arrays. Since RIE damage can affect MTJ performance, we checked the basic properties of the MTJs including TMR (tunneling magneto-resistive) ratio and RA (resistance–area) product. However, the MTJ test pattern has some parasitic components such as bottom and top contact resistances. In order to exclude these parasitic resistances from the overall resistance of MTJ test patterns, we measured the resistances of MTJs with and without the MgO barrier layer and then extracted the actual MTJ resistance. Figure 4 shows the extracted RA values for various MTJ dimensions. Since the RA was maintained at a constant value of ~30ohm*um^2 for the given MTJ dimensions, any shunting or edge damage due to MTJ RIE and post processes must be minimal.

Figure 5 shows typical R-H and R-V loops for our MTJs. For the more symmetric R-H loop in figure 5(b), the coercivity H_c is ~100Oe and the TMR is ~100%. While the negative shift of the R-H loop in figure 5(a) could give some advantage in write 1 (parallel to anti-parallel switching) operation margin and read-disturbance, switching instability in the R-V loop is observed due to lack of thermal stability. Figure 6 shows the key write current switching performance of our MTJs. The write currents I_{c0-} and I_{c0+} of 54x108nm MTJs are ~ -100μA (write current density J_{c0-} ~1.9MA/cm^2) and ~80uA (J_{c0+} ~ 1.5MA/cm^2), respectively. The write voltages V_{c0-} and V_{c0+} are ~-0.75V and ~0.65V, respectively. These V_{c0} values are relatively high due to the measured RA and J_{c0} values being higher than target. In the future, RA and J_{c0} will be improved through use of thinner MgO and DMTJ (dual barrier MTJ) structures. The thermal stability factor Δ of our MTJs was also measured to be ~57 by statistical analysis of the H_c variation [9], as shown in figure 7.

The write operation conditions and the load line characteristics of the cell transistor and MTJ are described in figure 8. From the load line characteristics, the cell transistor can provide sufficient current to switch the connected MTJ even considering the parasitic resistance effect and the core transistor variation in our system. We investigated the STT-RAM scalability through the scaling trends of the cell transistor and MTJ in our system. As shown in figure 9, the required MTJ switching current decreases more rapidly than the cell current drivability with device scaling. We expect that a 6~8F^2 cell dimension with single access transistor will be sufficient for MTJ switching at technology nodes below 30nm.

Memory bit cell array operation & chip design

We directly measured the bit cell resistances of each cell within a 64kbit test array with some circuit modification that involved bypassing the sense amplifier as shown in figure 10(a). We investigated the distribution of R_{High} and R_{Low} at the initial state in the 64kb cell array. Due to the good R-H symmetry, the R_{High} and R_{Low} distributions at the initial states are both present and can be separated from each other as shown in figure 10(b).

We characterized the switching performance of bit cell arrays in our test block. Figure 11 shows the switching current distribution for write operations and the path resistance distribution for R_{High} and R_{Low} in the test block. Due to good control of both the MTJ film deposition and the patterning process, the switching currents have a narrow distribution of 6σ /median < 50%. In addition, the number of shunted or stuck dies in the test block is very small, as seen from the path resistance distribution, so the switching yield in both directions is excellent.

We designed a 64Mbit STT-RAM using the above MTJ and cell transistor technology. The chip photograph and key chip features are shown in figure 12 and table 1, respectively. There is a 64Mbit main cell block in the center of the chip and several 64kbit test blocks to the left and right of the chip. A simulation result of the write and read operations is shown in figure 13. For the present design, we expect very fast STT-RAM memory operation with an address access time (t_{ACS}) of less than 20ns for the read operation.

Conclusion

A 64Mbit STT-RAM was successfully integrated at the 54nm technology node. The compact bit cell of 14F^2 can provide large enough current drivability and stable in-plane MTJ performance. From the design simulation and scaling trends of the MTJ and cell transistor, STT-RAM should be considered as a promising candidate to replace existing DRAM.

References

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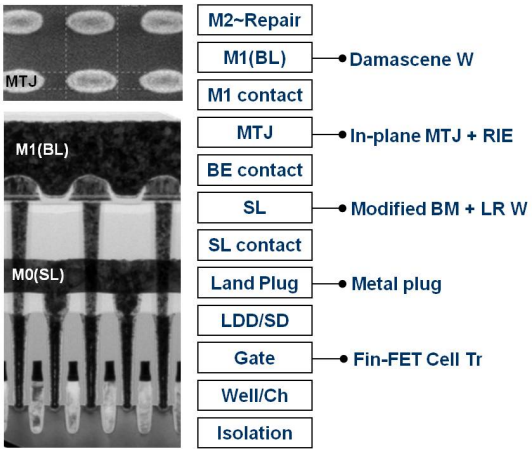

Figure 1 Top view of MTJ, TEM cross-section image and key process flow of STT-RAM at the 54nm technology node. The processes prior to BE contact are similar to a conventional DRAM process except for Fin-FET, metal

landing plug, and source line. The MTJ is located on the BE contact plug for high cell packing density.

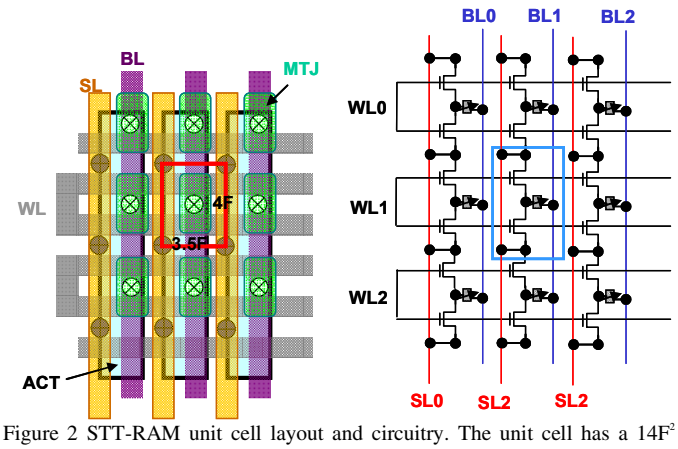

Figure 2 STT-RAM unit cell layout and circuitry. The unit cell has a $14F^2$ (WLxBL=3.5Fx4F), dual WL and SL//BL architecture.

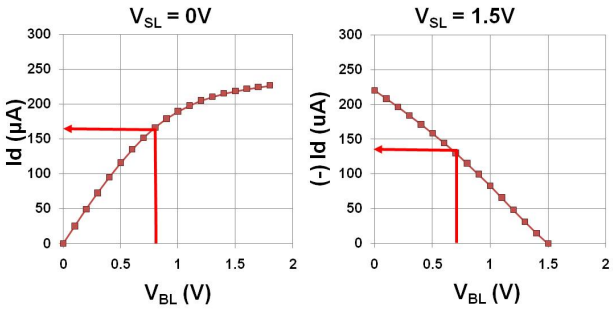

Figure 3 The current drivability of cell transistor with $14F^2$ for write 0 (BL=High) and write 1 (SL=High) operation. The red straight lines indicate the operation conditions for write 1 and write 0 in our system.

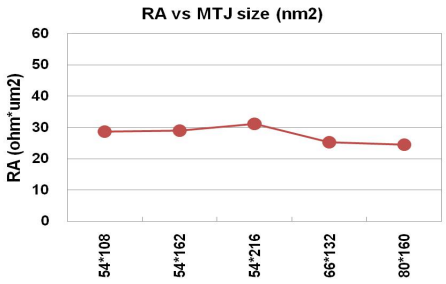

Figure 4 Measure RA product values at various MTJ dimensions.

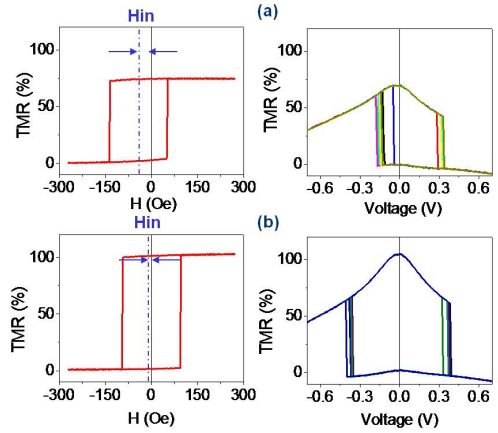

Figure 5 R-H and R-V loops of 54x108nm MTJs. (a) The MTJ device with large negative H_{in} (field offset) shows unrepeatable R-V switching during the write 1 (p → ap) operation. (b) The MTJ device with small Hin shows stable R-V switching in both directions. The extracted TMR value is ~100%.

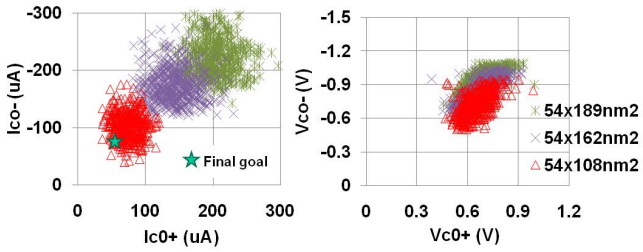

Figure 6 I_{c0} and V_{c0} for various MTJ aspect ratios. I_{c0} and V_{c0} are the calculated values at 10ns pulse width from the extrapolation of I_c vs pulse width in the ms region.

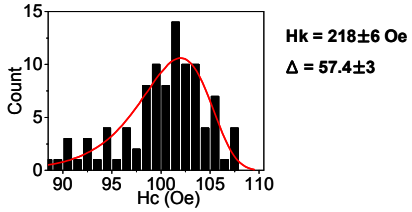

Figure 7 Hc distribution and calculated in-plane anisotropy field H_k and thermal stability Δ of the MTJ.

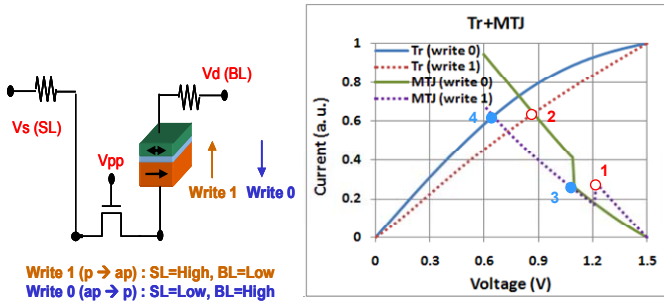

Figure 8 High bias is applied to SL for the write 1 (parallel state → anti-parallel state of MTJ) operation, while high bias is applied to BL for the write 0 (ap → p) operation. The load line characteristics show the cell current drivability margin for MTJ switching current in write 1 (p→ap) and write 0 (ap→p) operation in our system. The write 1 margin is the gap between the two open circles (1,2), while the write 0 margin is the gap between the two solid circles (3,4). Write 1 is harder than write 0 in terms of current drivability.

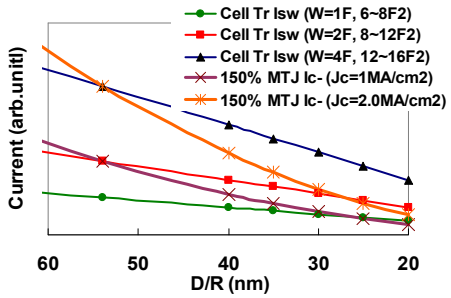

Figure 9 Forecast of STT-RAM scalability. Isw is the current drivability of the access cell transistor, while Ic is the required switching current of the MTJ. We assume that Isw should be larger than 150% × I_c to reflect the effects of external resistances and transistor skew.

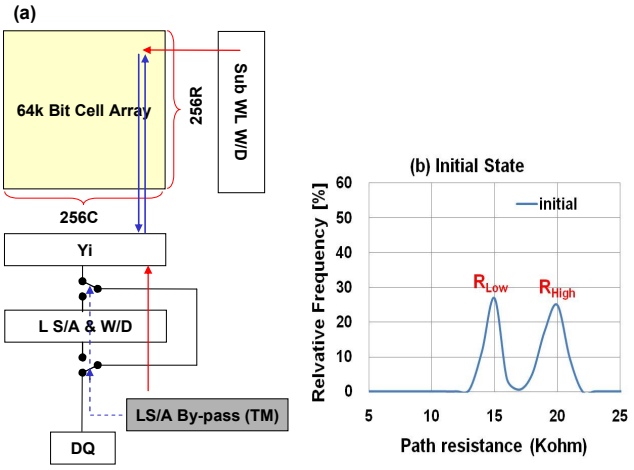

Figure 10 (a) Block diagram of direct access test mode for 64kbit cell array. (b) The R_{High} & R_{Low} distribution of bit cells (MTJ + cell transistor) for a 64k bit cell array in the initial state. R_{High} and R_{Low} are overlapped at the tail due to low TMR values in some dies. The value of Δ R / R for a 64kbit cell array is ~11.

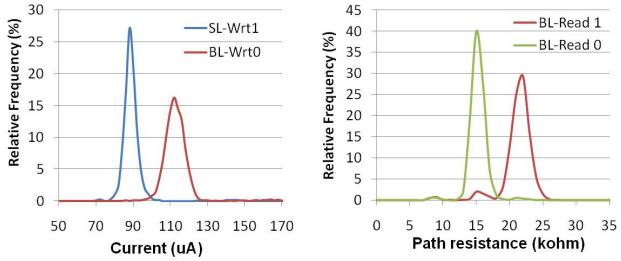

Figure 11 The switching current distribution for write operations and the path resistance distribution for R_{High} and R_{Low} in the test block.

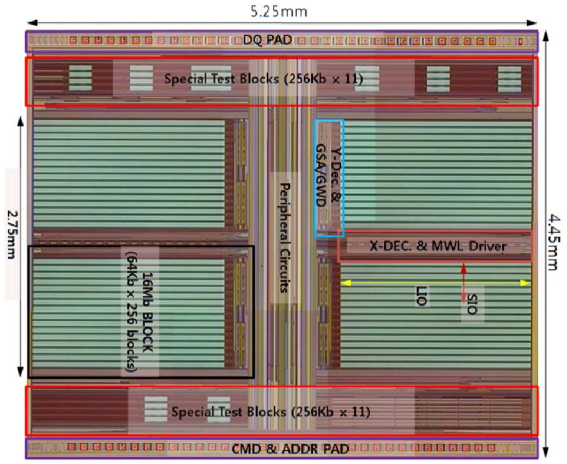

Figure 12 Micrograph of 64Mbit STT-RAM chip.

Table 1 Key features of 64Mbit STT-RAM chip.

Process	54nm CMOS, W SL & BL
Unit cell size	3.5Fx4F=14F^2 (0.188x0.216 = 0.041um^2)
# of Tr	2Tr / unit cell
MTJ	In-plane (54x108nm^2)
Chip density	64Mb (Org 4Mx16)
Chip size	4.45x5.25mm^2 (including 11 test blocks)
V_{DD}	1.8V

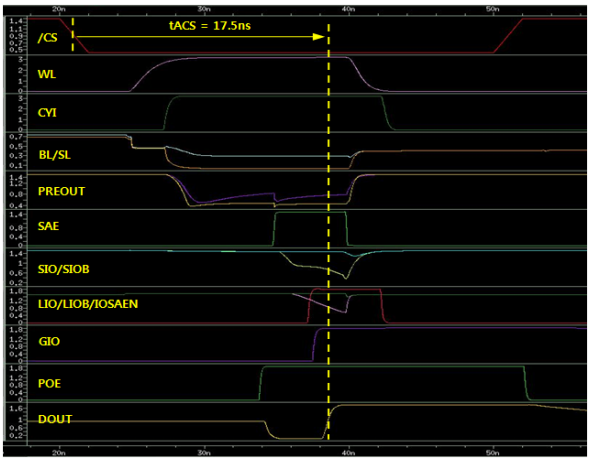

Figure 13 Simulation result of read operation of 64Mbit chip. The chip select access time, t_{ACS} is 17.5ns