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MRAM gets closer to the core

Improvements in magnetic tunnel junctions allows a 2 MB magnetic random-access memory array to be scaled for L4 cache applications.

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The development of fields such as machine learning and the Internet of Things is driving a revolution in computing hardware. These fields require memory that can store and retrieve large amounts of data in a fast and energy-efficient manner. In conventional computing systems, the gap in speed between processor and memory is one of the main bottlenecks in performance. Memory hierarchy, where memories are classified into different levels depending on their speeds and capacities (Fig. 1a) such as main memory or different levels of cache memory, can reduce this gap. However, conventional semiconductor technology-based memories such as static random-access memory (SRAM) and embedded dynamic random-access memory (eDRAM) are now struggling to meet the increasing demands in terms of energy efficiency, speed and density.

Magnetoresistive random-access memory (MRAM) is one alternative approach. The basic cell of MRAM is a magnetic tunnel junction (MTJ), which consists of a magnetic fixed layer, a non-magnetic tunnel barrier (usually magnesium oxide) and a magnetic free layer (Fig. 1b). The resistance state of the MTJ is determined by the relative magnetization direction between the fixed and the free layer, where a low (high) resistance state refers to the parallel (antiparallel) alignment of the magnetizations. By driving a current across the junction, the magnetization of the free layer can be switched via the spin-transfer torque (STT) effect. Binary information — 0s and 1s — can thus be stored as low- and high-resistance states in the MTJ.

STT-MRAM has gained interest in industry due to its non-volatility and compatibility with standard semiconductor technology, as well as its potentially fast operation speed, long endurance and high density. And recently, semiconductor companies, including Intel, Samsung, GlobalFoundries and TSMC, have demonstrated the feasibility of commercial embedded non-volatile memory (eNVM) based on STT-MRAM[1–4]. Reporting at the 2019 IEEE International Electron Devices Meeting in San Francisco, Juan Alzate and colleagues at Intel demonstrated a 2 MB STT-MRAM array that is capable of level 4 (L4) cache application[5].

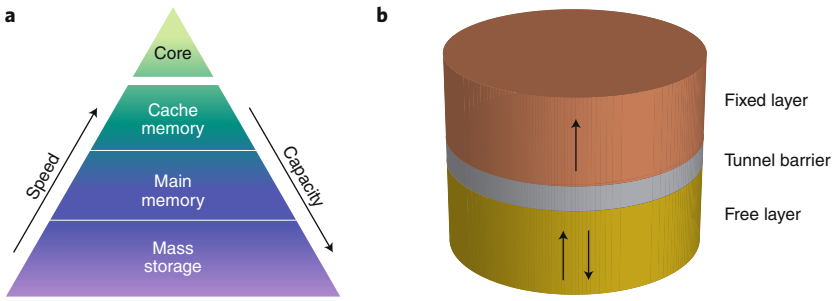

Fig. 1 | Memory hierarchy and MTJ. a, Schematic of memory hierarchy. The speed (capacity) is increased (decreased) for different levels of memories from the bottom to top. **b**, Schematic of an MTJ. The resistance state is determined by the relative magnetization direction (black arrows) between the fixed and the free layer. Magnetization of the free layer can be switched by driving a current across the junction.

In the memory hierarchy, L4 cache is not as fast as caches that are closer to the core, such as L1 or L2 cache, but it has larger capacity. Compared with eNVM, L4 cache imposes stricter requirements such as higher density, faster speed, lower bit error rate and better endurance. By finely optimizing the process to fabricate STT-MRAM arrays, the researchers were able to meet all these requirements. First, the array density needed to be improved in order to be placed on-chip, which requires a smaller transistor and MTJ size within a single memory cell (that is, a one-transistor–one-MTJ structure). However, a smaller transistor also limits the maximum writing current and could potentially affect the write error rate. Moreover, to achieve a faster writing speed, the write pulse duration needs to be reduced, which creates another challenge in order to meet an acceptable write error rate. With the optimized process, MTJs with a size smaller than 55 nm could be fabricated, which show acceptable write error rates for array-level operation and function over the proposed operating temperature range (−10 °C to 110 °C).

In terms of reliability, the frequent operation of cache requires a great endurance, but the corresponding retention time can be relaxed thanks to data scrubbing (in which the data are frequently checked and corrected to avoid accumulation of errors). STT-MRAM also suffers from read disturbance since the write and read operation share the same current path. During a read operation, the thermal fluctuation and the stochasticity of STT might induce an error operation by flipping the magnetization of the free layer. To address these reliability requirements, Alzate and colleagues tested the fabricated STT-MRAM arrays and reported a 1 s retention at 110 °C, an endurance of 10^{12} cycles, and an acceptable bit error rate ($<10^{-5}$) for read disturbance. All these characterizations illustrate that such STT-MRAM arrays are ready for an L4 cache application.

The demonstration of L4 cache-ready STT-MRAM should encourage further developments on STT-MRAM for other level memory applications. Pushing the performance and reliability of STT-MRAM is essential for the development of commercial products. However, it is also important to develop other aspects of MRAM. For example, exploring voltage-controlled writing schemes could improve the energy efficiency and density of

MRAM[6–8]. Also, the recently discovered spin–orbit torque[9,10] could potentially endow faster switching speed and better endurance to MRAM due to the different switching mechanism and separated write and read paths. These novel working schemes could further enrich the tunability of MRAM and make it a more versatile memory technology, which covers a range of memory applications and may even lead to spin-based core logic units. ❐

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