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Emerging Memory Technologies

Recent Trends and Prospects

This tutorial introduces the basics of emerging nonvolatile memory (NVM) technologies including spin-transfer-torque magnetic random access memory (STT-MRAM), phase-change random access memory (PCRAM), and resistive random access memory (RRAM). Emerging NVM cell characteristics are summarized, and device-level engineering trends are discussed. Emerging NVM array architectures are introduced, including the one-transistor–one-resistor (1T1R) array and the cross-point array with selectors. Design challenges such as scaling the write current and minimizing the sneak path current in cross-point array are analyzed. Recent progress on megabit- to gigabit-level prototype chip demonstrations is summarized. Finally, the prospective applications of emerging NVM are discussed, ranging from the last-level cache to the storage-class memory in the memory hierarchy. Topics of three-dimensional (3D) integration and radiation-hard NVM are discussed. Novel applications beyond the conventional memory applications are also surveyed, including physical unclonable function for hardware security, reconfigurable routing switch for field-programmable gate array (FPGA), logic-in-memory and nonvolatile cache/register/flip-flop

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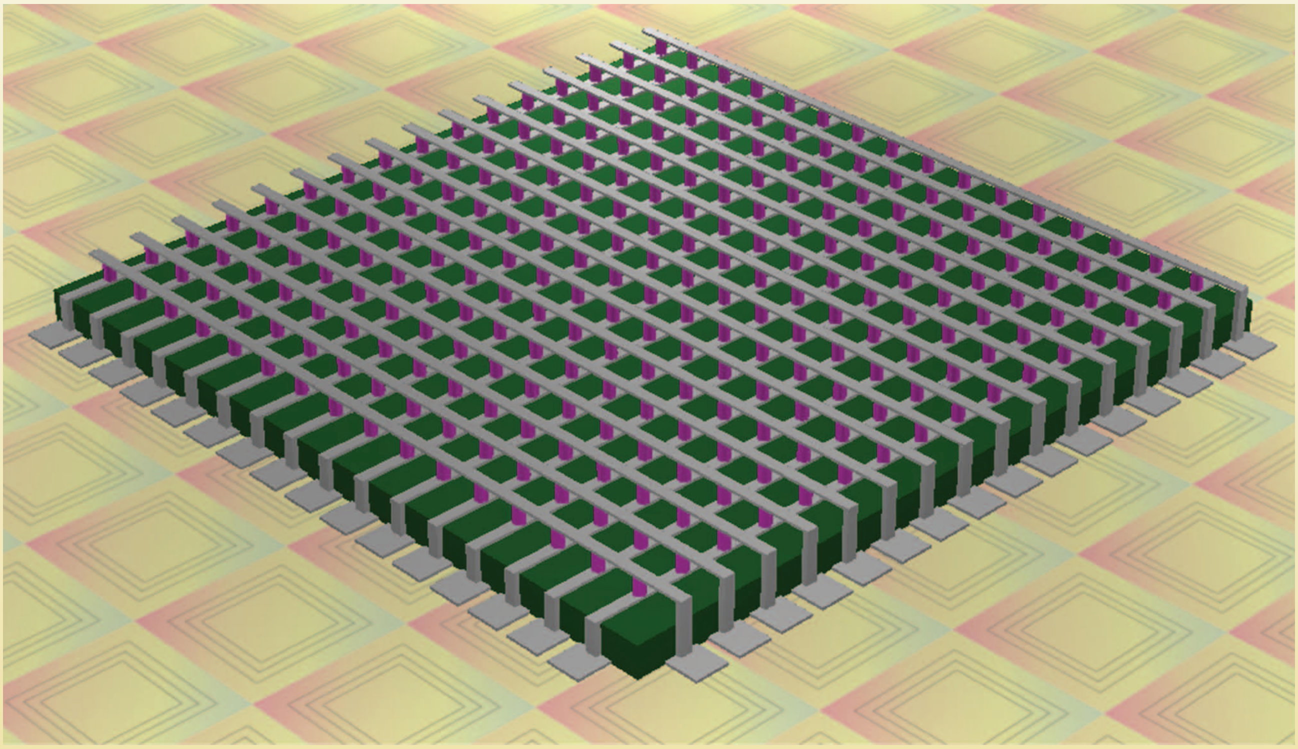

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for nonvolatile processor, and synaptic device for neuro-inspired computing.

Overview of Emerging Memory Technologies

The functionality and performance of today's computing system are increasingly dependent on the characteristics of the memory subsystem. The memory subsystem has a well-known memory hierarchy: Today static random-access memory (SRAM), dynamic random-access memory (DRAM), and flash are the mainstream memory technologies serving as cache, main memory, and storage memory such as solid-state drive (SSD), respectively. Moving up the memory hierarchy toward the cache, the memory write/read latency decreases. Moving down the memory hierarchy toward the storage, the memory capacity increases. These mainstream memory technologies are essentially based on the charge storage mechanism: SRAM stores the charges at the storage nodes of the cross-coupled inverters, DRAM stores the charges at the cell capacitor, and flash stores the charges at the floating gate of the transistor. All these charge-based memories face challenges in scaling down to the 10-nm node and beyond. The easy loss of the stored charges at nanoscale results in the degradation of performance, reliability, and noise margin. In this context, emerging memory technologies that are noncharge based are actively under research and development in the industry, with the hope of revolutionizing the memory hierarchy [1].

The ideal characteristics for a memory device include fast write/read speed (<ns), low operation voltage (<1 V), low energy consumption (~fJ/b for write/read), long data retention time (>10 years), long write/read cycling endurance (>10^{17} cycles), and excellent scalability (<10 nm). Nevertheless, it is almost impossible to satisfy all of these ideal characteristics in a single "universal" memory device. Several resistance-based emerging NVM technologies have been pursued toward achieving part of these ideal characteristics. The emerging NVM candidates include STT-MRAM [2], PCRAM [3], and RRAM [4].

These emerging NVM technologies share some common features: they are nonvolatile two-terminal devices, and they differentiate their states by the switching between a high resistance state (HRS, or off state) and a low resistance state (LRS, or on state). The switching from off state to on state is called "set," and the switching from on state to off state is called "reset." The transition between the two states can be triggered by an electrical stimulus (i.e., voltage or current pulse). However, the detailed switching physics is quite different: STT-MRAM relies on the parallel configuration (corresponding to LRS) and antiparallel configuration (corresponding to HRS) of two ferromagnetic layers separated by a thin tunneling insulator layer; PCRAM relies on chalcogenide materials to switch between the crystalline phase (corresponding to LRS) and the amorphous phase (corresponding to HRS); and RRAM relies on the formation (corresponding to LRS) and the rupture (corresponding to HRS) of conductive filaments in the insulator between two electrodes. Table 1 compares the typical device characteristics of the emerging memory technologies and the mainstream memory technologies.

Due to the different underlying physics, the device characteristics are also different among emerging NVMs. Therefore, different emerging NVMs may have different application spaces due to their unique characteristics. As compared to SRAM, STT-MRAM has an advantage of a smaller cell area, while STT-MRAM has maintained low programming voltage, fast write/read speed, and long endurance. Thus, STT-MRAM is attractive as a replacement for embedded

TABLE 1. DEVICE CHARACTERISTICS OF MAINSTREAM AND EMERGING MEMORY TECHNOLOGIES.

	MAINSTREAM MEMORIES				EMERGING MEMORIES		
			FLASH				
	SRAM	DRAM	NOR	NAND	STT-MRAM	PCRAM	RRAM
Cell area	>100 F^2	6 F^2	10 F^2	<4F^2 (3D)	6~50F^2	4~30F^2	4~12F^2
Multibit	1	1	2	3	1	2	2
Voltage	<1 V	<1 V	>10 V	>10 V	<1.5 V	<3 V	<3 V
Read time	~1 ns	~10 ns	~50 ns	~10 µs	<10 ns	<10 ns	<10 ns
Write time	~1 ns	~10 ns	10 µs–1 ms	100 µs–1 ms	<10 ns	~50 ns	<10 ns
Retention	N/A	~64 ms	>10 y	>10 y	>10 y	>10 y	>10 y
Endurance	>1E16	>1E16	>1E5	>1E4	>1E15	>1E9	>1E6~1E12
Write energy (J/bit)	~fJ	~10fJ	~100pJ	~10fJ	~0.1pJ	~10pJ	~0.1 pJ

Notes: F: feature size of the lithography. The energy estimation is on the cell-level (not on the array-level). PCRAM and RRAM can achieve less than 4F^2 through 3D integration. The numbers of this table are representative (not the best or the worst cases).

memories (e.g., SRAM or embedded DRAM) in the last-level cache [5]. As compared to flash, PCRAM/RRAM is attractive due to its lower programming voltage and faster write/read speed. Thus, the PCRAM/RRAM is attractive as a replacement for NOR flash for code storage and, more ambitiously, to replace NAND flash for data storage [6]. Besides replacing the existing technologies, the emerging NVM technologies hold the potential to revolutionize today's memory hierarchy by adding more levels in the hierarchy, e.g., creating a storage-class memory layer between the main memory and the SSD [7]. In addition, hybrid systems with emerging memories and mainstream memories are also attractive, e.g., using RRAM as the cache for NAND flash [8].

Emerging NVM Cell Structures and Device-Level /Engineering Challenges

Despite the aforementioned attractive features, emerging NVM technologies face challenges from aspects of process compatibility, manufacturing yield, performance variability, and reliability. In the following, we will discuss the challenges and recent trends of each NVM candidate at the device level.

STT-MRAM Cells

STT-MRAM is based on the magnetic tunnel junction (MTJ) structure. The tunneling magnetoresistance (TMR) ratio (defined as $R_{ap}/R_p - 1$) of the MTJ is typically small (<200% or <2X), thereby imposing challenges for sensing circuit design to sense the small difference between the on and off states. It is also well known that a tradeoff exists between the thermal stability (E_a/kT) and critical write current density (J_c) due to an energy barrier between the parallel and antiparallel states of the MTJ. Given the application demands, the data retention requirement may be relaxed to reduce the write power, e.g., for the last-level cache in which the data are frequently updated. The current trend of STT-MRAM cell design is to switch from the in-plane MTJ [Figure 1(a)] to the perpendicular MTJ [Figure 1(b)] to allow better scalability, longer retention, and lower J_c [9], [10]. The in-plane MTJ's scalability is limited by the aspect ratio (length/width in the lateral dimension) of the cell, as a sufficient shape anisotropy is required for thermal stability, while

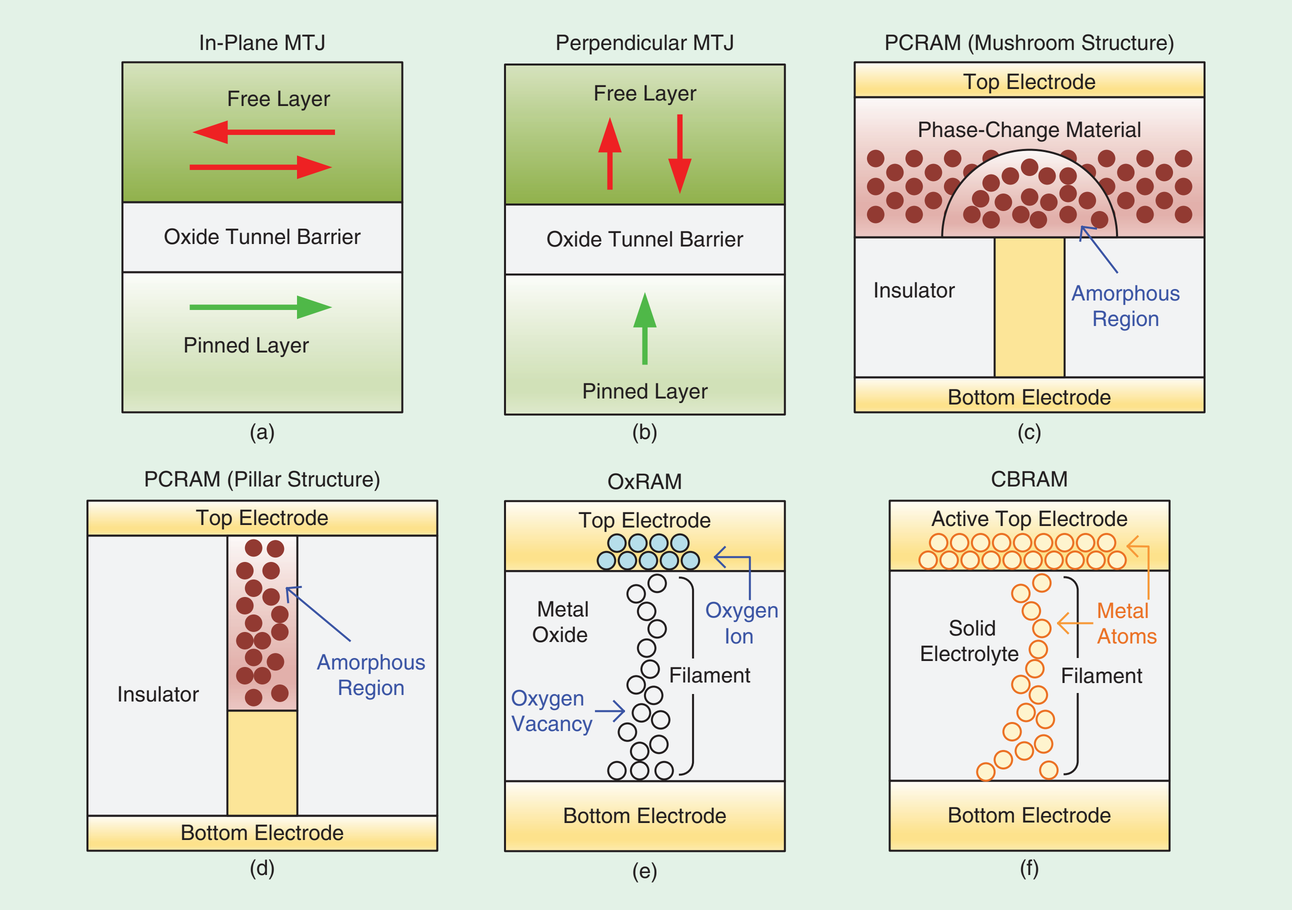

FIGURE 1: A schematic of emerging NVM device structures. (a) STT-MRAM with in-plane MTJ structure. (b) STT-MRAM with perpendicular MTJ structure, which allows better scalability. (c) PCRAM with mushroom structure. (d) PCRAM with thermally confined pillar structure for reducing write current. (e) RRAM based on oxygen vacancies in the filament in the oxide, referred to as OxRAM. (f) RRAM based on metal ions diffusion from active electrode to form conductive bridge in solid electrolyte, referred to as CBRAM.

the perpendicular MTJ achieves the shape anisotropy in the vertical dimension, allowing better scalability in the lateral dimension. State-of-the-art perpendicular MTJ cells have been scaled to 15 nm [11], [12].

Today STT-MRAM's process and manufacturing technology are relatively mature. However, STT-MRAM has relatively poor process compatibility with mainstream silicon CMOS technology, because more than ten layers of exotic ferromagnetic materials (typically CoFeB/MgO) are used in the MTJ stack. In addition, keeping within the thermal budget to crystallize all the magnetic layers while maintaining downward CMOS doping profiles is challenging. The precise deposition and etching to avoid the formation of dead layers/regions of the complicated MTJ stack add another significant cost barrier for foundries to widely adopt this technology.

The functionality and performance of today's computing system are increasingly dependent on the characteristics of the memory subsystem.

PCRAM Cells

The PCRAM cells are typically based on GST materials (e.g., $Ge_2Sb_2Te_5$). The GST material systems can further be tuned for device characteristics that are of interest. For example, Ge-rich GST (*N*-doped) could be used to achieve better data retention for high temperature automotive applications [13]. The PCRAM's on/off resistance ratio is much larger (in the range of 100–1,000×) than STT-MRAM. Thus, in principle, multilevel cell (MLC) operations are allowed (even 4 b/cell are feasible [14]). The key challenge for PCRAM cell design is the relatively large write current required to melt the phase-change materials. Even for state-of-the-art PCRAM at 20 nm, the write current (~100 μA [15]) is roughly three to ten times larger than its STT-MRAM or RRAM counterparts. The current trend of PCRAM cell design is to switch from the mushroom cell [Figure 1(c)] to the pillar cell [Figure 1(d)] to confine the heat dissipation, thereby reducing the write current. An extremely scaled PCRAM cell using the carbon-tube electrodes suggests that the write current can achieve ~1 μA at 2-nm node [16]. The PCRAM's switching speed (>50 ns) is limited by the slow crystalline process, also ten times longer than its RRAM counterparts, while the PCRAM's endurance (10^6~10^9 cycles) is comparable to that of the RRAM. The PCRAM's data retention (especially for the MLC) is limited by resistance drift due to the relaxation of the amorphous state. Thus, sophisticated circuit-level compensation schemes are needed [17]. Despite the fact that the PCRAM's cell characteristics are less competitive than RRAM in terms of the write power and speed, today PCRAM's process and manufacturing technology is quite mature. PCRAM has generally good process compatibility with mainstream silicon CMOS technology, as GST materials can be deposited by sputtering under back-end-of-line (BEOL) temperature (<400 °C).

RRAM Cells

There are two subcategories within RRAM: oxide-RAM (OxRAM) and conductive bridge RAM (CBRAM). The difference is that OxRAM's filament consists of oxygen vacancies in the oxide layer [Figure 1(e)], while CBRAM's filament consists of metal atoms, formed by fast-diffusive Ag or Cu ions migrating into the solid-electrolyte [Figure 1(f)]. Despite different underlying physics, these two types of RRAMs share many common device characteristics. The only notable difference may be that OxRAM's on/off resistance ratio may be smaller (in the range of 10–100×) and offers better endurance up to 10^{12} cycles, while CBRAM's on/off resistance ratio can be quite large (10^3–10^6×) but with limited endurance (<10^4 cycles) [18]. The switching of RRAM includes unipolar and bipolar modes depending on the oxide and electrode materials system [19]. The unipolar mode generally requires larger write current and shows less endurance; thus, the bipolar mode is preferred. The key challenge of RRAM cell design is the variability of the switching parameters. Owing to the stochastic nature of ionic (oxygen vacancies or metal ions) migration, the filament shape varies from device to device and also from cycle to cycle (within one device). Remarkable variation in resistance distribution (which can be one or two orders of magnitude) adds challenges to the sensing circuit design and requires the write-verify techniques to program to the target states, which could be latency consuming for the MLC operations. Although RRAM could require smaller write current (e.g., ~10 μA) due to the filamentary switching mechanism, the data retention may be problematic when filament is too thin [20], and at the same time the random telegraph noise due to the filament instability may become significant [21]. Nevertheless, the scalability to 2-nm node of RRAM cell has been demonstrated by sidewall electrodes [22]. RRAM has generally excellent process compatibility with the mainstream silicon CMOS technology, as many RRAM materials (e.g., HfO_x, TaO_x) are already used in silicon transistors' high-*k* dielectric process. Atomic-layer deposition allows for the accurate deposition of RRAM thin film under BEOL temperature (<400 °C).

Emerging NVM Array Architectures and Circuit-Level Design Challenges

1T1R Array Architecture

One of the common emerging NVM array architectures is the 1T1R array.

In this design, each NVM cell is in series with a cell selection transistor, as shown in Figure 2(a). The addition of a selection transistor is able to isolate the selected cell from other unselected cells. The word line (WL) controls the gate of the transistor; thus, tuning the WL voltage can control the write current that is delivered to the NVM cell. The NVM cell's top electrode connects to the bit line (BL) while its bottom electrode connects to the contact via to the drain of the transistor. The source line (SL) connects to the source of the transistor. The typical cell area of 1T1R array is 12 F^2 (F is the lithography feature size) if the gate width/length (W/L) of the transistor is one. The minimum cell area can be reduced to 6 F^2 if the aggressive borderless DRAM design rule with sharing BL and SL is applied. The cell area will be increased if the W/L of the transistor is larger than one when a minimum-sized transistor cannot provide sufficient write current (usually in cases of STT-MRAM and PCRAM).

Figure 2(a)–(c) shows the typical write/read scheme for the 1T1R array. For the set operation, WL voltage is applied to turn on the transistor of the selected cell, and a write voltage is applied to the BL of the selected cell while SL is grounded; for the reset operation, WL voltage is applied to turn on the selection transistor of the selected cell, and a write voltage is applied to the SL of the selected cell while BL is grounded to reverse the current, as the typical STT-MRAM and RRAM operation needs "bipolar" switching (PCRAM does not need to reverse the voltage polarity though). For unselected rows and columns, the WL, BL, and SL are all grounded. To read out the data from the 1T1R array, WL voltage is applied to turn on the selection transistor of the selected cell, and a read voltage is applied to the BL while SL is grounded. The sense amplifier (S/A) thus can sense the difference in the read-out current for HRS and LRS through the BL with a reference. Because the transistors are off for the unselected cells, there are no crosstalk or interference issues in the 1T1R array, and each cell can be independently and randomly accessed. Multiple bits can be written (or read) in parallel into (or from) the same row by activating multiple columns.

The 1T1R array faces scaling challenges if the NVM's write current cannot scale accordingly. Figure 2(d) shows the silicon CMOS low-power logic transistor's drive current with the scaling from 130 nm down to 20 nm for different W/L simulated with the Predictive Technology Model (PTM) [23]. The representative write current of STT-MRAM, PCRAM, and RRAM from the literature data is also marked. RRAM's write current typically ranges from 10 to 100 µA (with some scattered data points for sub-10 µA), and it does not scale with the device area due to the filamentary conduction mechanism. Although STT-MRAM and PCRAM's write current scales with the device area, at 20-nm node, STT-MRAM's current is ~40 µA, and PCRAM's current is ~100 µA. It is seen that in most cases, $W/L = 1$ transistors could not provide sufficient write current for a NVM cell; thus, 6 F^2 cell area is unlikely to achieve using logic-compatible process. Although the transistor's gate voltage (V_{gs}) can be boosted under the specially engineered DRAM process to increase the drive current, it is still limited. For example, the drive current at V_{gs} = 5 V can approach 40 µA for a $W/L = 1$ transistor at 27-nm node [24]. Therefore, reducing the write current down to sub-10 µA by device engineering is of great importance for continuing the scaling of the 1T1R array. In addition, reducing the write voltage down to sub-1 V is also necessary for embedded applications if using a logic-compatible process.

Cross-Point Array Architecture

The other common array architecture is the cross-point (X-point, or crossbar) array, which consists of

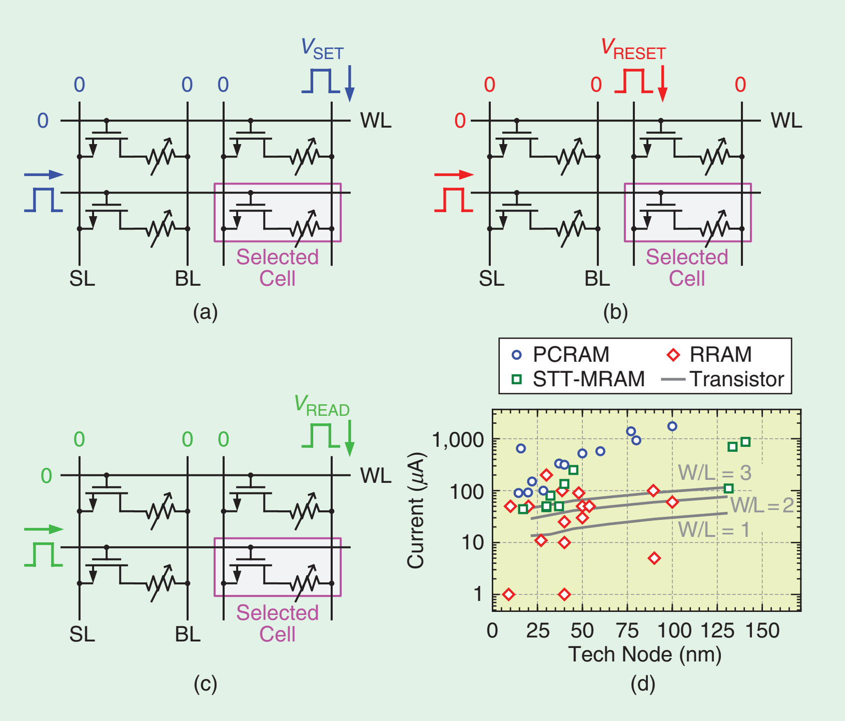

FIGURE 2: A schematic of the 1T1R array: (a) set scheme, (b) reset scheme, and (c) read scheme. (d) A silicon CMOS low-power logic transistor's drive current with the scaling from 130 nm down to 20 nm for different W/L simulated with the PTM model [23]. The representative write current of STT-MRAM, PCRAM, and RRAM from the literature data is also marked.

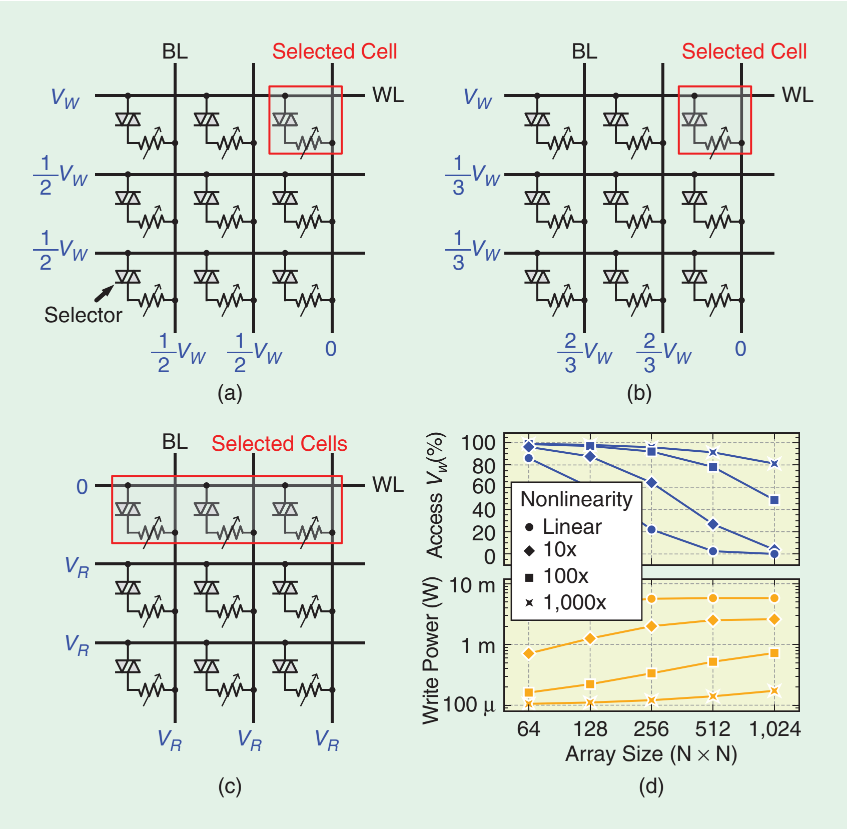

FIGURE 3: A schematic of the cross-point array. The selector is added in series with the RRAM cell at each cross-point. (a) V/2 write scheme. (b) V/3 write scheme. (c) Read scheme (for an entire row). (d) SPICE simulation of write margin and write power as a function of cross-point array size. Increasing the NVM cell's I-V nonlinearity (*N*) by adding selectors is helpful to minimize the IR drop problem along the interconnect wire and the sneak path problem.

rows and columns perpendicular to each other with NVM cells sandwiched in between, as shown in Figure 3(a). The cross-point array, in principle, can achieve a 4 F^2 cell area; thus, it can achieve higher integration density than the 1T1R array. Typically, the selectors are added in series with the NVM cells to prevent cross talk or interference between cells in the cross-point array, which is referred to as one-selector and one-resistor (1S1R) architecture. The cross-point array can support PCRAM and RRAM but generally does not support STT-MRAM because of a very small on/off ratio (~2×); thus, the sense margin becomes indistinguishable due to the sneak path current.

The write/read schemes of the cross-point array are as follows. To successfully program the NVM cells, two common write schemes (V/2 and V/3) can be applied. Figure 3(a) shows the voltage bias conditions for the V/2 scheme. In the V/2 scheme, for the set operation, the selected cell's WL and BL are biased at the write voltage V_w and ground, respectively. For the reset operation, the bias conditions on WL and BL are reversed for the bipolar switching. In both set and reset operations, all the unselected WLs and BLs are biased at $V_w/2$. Therefore, only the selected cell sees a full V_w, while the half-selected cells along the selected WL or BL see a half V_w and all the other unselected cells in the array see zero voltage [in reality, due to the current-resistance (IR) drop along the interconnect, the voltage is not perfectly zero though]. Here the assumption is that $V_w/2$ should not disturb the half-selected cell's resistance. Figure 3(b) shows the voltage bias conditions for the V/3 scheme. In the V/3 scheme, for the set operation, the selected cell's WL and BL are biased at the write voltage V_w and ground, respectively. For the reset operation, the bias conditions on WL and BL are reversed for the bipolar switching. The unselected WLs and BLs are biased at 1/3 V_w and 2/3 V_w for the set operation, respectively. The unselected WLs and BLs are biased at 2/3 V_w and 1/3 V_w for the reset operation, respectively. In this way, the selected cell sees V_w, while all other unselected cells in the array only see 1/3 V_w. Here the assumption relaxes so that 1/3 V_w should not disturb the unselected cell's resistance. The pros and cons of these two write schemes can be summarized as follows: the V/2 scheme typically has less power consumption than the V/3 scheme. This is because the unselected cells (not along the selected WL and BL) in the V/2 scheme see zero voltage ideally, while all the unselected cells in the V/3 scheme see 1/3 V_w, thus consuming static power during the write period. On the other hand, the V/3 scheme has better immunity to the write disturbance than the V/2 scheme, as the maximum voltage that the unselected cells see is 1/3 V_w in the V/3 scheme while is 1/2 V_w in the V/2 scheme. It is possible to have multiple-bit parallel write in the cross-point array with either the V/2 or V/3 scheme by biasing multiple BLs (or WLs) to be ground in the set (or reset) operation. The penalty for multiple-bit parallel write is a larger driver size at each row (or column) as it has to deliver the multiple write current in addition to the sneak path via the unselected cells. Figure 3(c) shows the read scheme for the cross-point array. All the columns are biased at the read voltage V_r, while the selected row is biased at ground and the unselected rows are biased at V_r. Therefore, only the cells of the selected row see a read voltage and all the other unselected cells see zero voltage (in reality, due to the IR drop along interconnect, the voltage is not perfectly zero though). The entire selected row can be read-out in parallel if each column can have one S/A. However, the pitch of S/As is typically larger than the column pitch; thus, multiple columns have to share one S/A. S/As can be generally categorized into two types [25]: voltage mode and current mode. In practical designs, the choice between voltage-mode sensing and current-mode sensing depends on the array size and the NVM cell characteristics. The general conclusion is that for an array with a long BL length or a higher LRS resistance (smaller read-out current), current sensing provides faster access.

The cross-point array suffers from two well-known design challenges: 1) the IR drop problem along the interconnect wire and 2) the sneak path problem through the unselected cells. The IR drop problem becomes significant when the WL and BL wire width scales to sub-50-nm regime where the interconnect resistivity drastically increases due to the increased electron surface scattering. For example, at 20-nm node, the copper interconnect resistance between two neighboring cells is ~2.93 Ω; thus, the IR drop along the wire for a large array (e.g., a 1,024 × 1,024 array) is no longer negligible. The farthest cell from the driver sees an interconnect resistance ~3 kΩ. If the NVM cell's resistance (typically a few kΩ up to tens of kΩ) is comparable to this interconnect resistance, a portion of the write voltage will drop on the wire instead of the NVM cell. To guarantee a successful write operation, the write voltage provided from the driver has to be boosted over the actual switching voltage of the NVM cell to compensate for the IR drop. However, the write voltage cannot be boosted too much because 1/2 V_w (in the V/2 scheme) should not disturb the NVM resistance for the cells close to the driver.

The sneak path problem is associated with the IR drop problem. Take the V/2 scheme as an example. The half-selected cells along the selected WL and BL form the sneak paths during the write operation. The sneak paths contribute additional current to the IR drop and further degrade the write margin. Meanwhile, the sneak paths increase the write current (thus the write power) that is provided by the driver transistors at the edge of the cross-point array. Further discussions about the IR drop problem and the sneak path problem of the cross-point array architecture can be found in [26]–[28]. The conclusions from these works indicate that increasing the LRS resistance (or equivalently reducing the write current) and increasing the I–V nonlinearity of the NVM cell (with the help of the selector) are useful to minimize the IR drop and sneak paths. Figure 3(d) shows the SPICE simulation of the write margin and write power as a function of the cross-point array size for different I–V nonlinearity (N). The nonlinearity is defined as the current ratio between V_w and $V_w/2$. The NVM cell resistance is fixed at 40 kΩ, and the wire width is fixed at 20 nm in this study. It is seen that at least $N > 1{,}000$ is needed for maintaining sufficient write margin and minimizing write power for a large array (e.g., a 1,024 × 1,024 array).

Selector Device for Cross-Point Array

Next we will survey the two-terminal selector devices reported in [29]. For unipolar switching (e.g., PCRAM), a p-n diode is the most common device for the cell selector. Although a high-performance p-n diode is easily fabricated with epitaxial silicon technology for the planar device structure, it is not feasible to implement an epitaxial silicon-based p-n diode at the BEOL for 3D integration because it is difficult to grow epitaxial silicon on a metal layer and a high processing temperature is required. On the other hand, amorphous silicon allows for a BEOL processing temperature (<400 °C). But an amorphous silicon p-n diode does not meet the requirement for the current density for the NVM programming. For bipolar switching (e.g., RRAM), bidirectional nonlinearity is required (note: a bidirectional selector also works for unipolar PCRAM).

There are two types of bidirectional selectors: Type I: exponential I–V and Type II: threshold I–V. Figure 4(a) and (b) shows the representative I–V

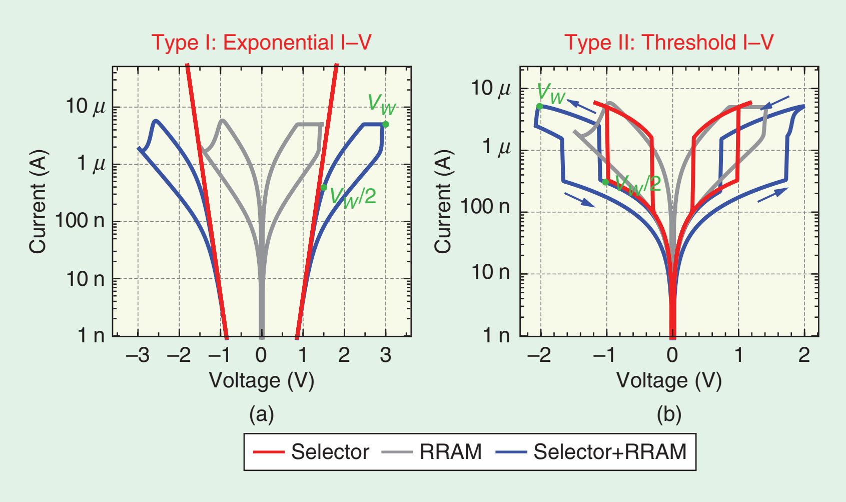

FIGURE 4: Representative I-V characteristics for a bipolar RRAM with (a) Type I selector and a bipolar RRAM with (b) Type II selector. SPICE simulation is performed with the RRAM compact model [38].

characteristics for a bipolar RRAM with Type I selector and a bipolar RRAM with Type II selector, respectively. The metrics of selector performance are 1) the nonlinearity (N) defined as the current ratio between V_w and $V_w/2$, which will determine how effective the sneak current suppression is, and 2) the drive current density (e.g., 10 MA/cm^2 is required for 10-μA write current at the 10-nm node). Oxide/electrode interface engineering or oxide/oxide bandgap engineering with the tunneling current mechanism can be leveraged as Type I selector, e.g., Ni/TiO$_2$/Ni bidirectional selector [30]. In addition, Cu ion motion in the Cu-containing mixed-ionic-electronic-conduction materials also show a good bidirectional exponential I–V for bipolar switching RRAM, as demonstrated by a series of works [31]–[33]. The aforementioned Type I selectors rely on an exponential slope in the I–V curve to turn on the selector, accompanied with an increase of the current by several orders of magnitude. Ideally, an abrupt turn-on behavior with steep slope is preferred, which is referred to as the threshold switching (Type II). The threshold selector typically exhibits a hysteresis in I–V as it turns on above a threshold voltage and turns off below a hold voltage. Threshold switching can be achieved in the metal-insulator-transition (MIT) Mott oxide materials such as NbO$_2$ [34]. The drawback of MIT-based threshold selectors is a relatively small nonlinearity (typically $N < 100$). Besides Mott oxide materials, an ovonic-threshold-switch based on chalcogenide materials has been demonstrated to be an excellent threshold selector [35]. Recently, a field-assisted-superlinear-threshold selector has been reported [36], which shows outstanding nonlinearity ($N > 10^7$), steep turn-on slope (<5 mV/dec) and high current drivability (>5 MA/cm^2), and the threshold voltage is claimed to be adjustable from ~0.3 V to ~1.3 V to match various RRAM characteristics.

Although substantial progress has been made in the past few years, the development of selector devices is still a key challenge for implementing large-scale cross-point memory architectures today. Most importantly, the selector device characteristics must match the NVM device characteristics. Adding selector devices in series with the NVM cell inevitably increases the programming voltage as part of the voltage is used to turn on the selector device. For the bidirectional selector with exponential I–V, the read sense margin generally degrades because the read-current for LRS is also suppressed. As a result, it requires a much longer time for sensing. As a reference, a well-designed current-mode sense amplifier can sense sub-100 nA read-out current within 26 ns [37]. For the threshold switching selector with abrupt I–V, the read voltage has to be boosted above the threshold voltage of the selector; thus, it runs a risk of disturbing the NVM resistance in the read operation. Ultimately, it is preferred that the NVM cell itself has a built-in I–V nonlinearity thereby eliminating the necessity of the external selector device.

Merging NVM technologies face challenges from aspects of process compatibility, manufacturing yield, performance variability, and reliability.

Recent Progress on Prototype Chip Demonstration

There are two methods for integrating RRAM cells on top of the CMOS circuits. The first approach is to fabricate the RRAM cells following the front-end-of-line process (close to the transistor fabrication at a lower-level interconnect). For example, the RRAM cells can be deposited at the contact via between the drain and metal 1, and this approach is typically employed in the 1T1R array architecture. The second approach is to fabricate the RRAM cells via the BEOL process at the top-level interconnect (decoupled from the transistor fabrication). For example, the RRAM cells can be deposited at the contact via between metal 4 and metal 5. One of the advantages of the BEOL integration is that the peripheral circuits can be hidden underneath the cross-point array to save the area as demonstrated in Panasonic's 8-Mb prototype chip [39].

Figure 5 summarizes the recent prototype chip demonstrations of various NVM technologies reported in the major conferences. Figure 5(a) shows the memory capacity versus year, and Figure 5(b) shows the write/read bandwidth versus year. PCRAM and RRAM have demonstrated >Gb-level capacity owing to the smaller cell size (4 F^2 using cross-point array or 6 F^2 using 1T1R array with minimum sized transistor), while STT-MRAM's capacity is only up to the 64-Mb level (cell size is still >30 F^2 owing to a larger transistor used to deliver sufficient write current in the 1T1R array and a relaxed layout design rule). It is noted that the bandwidth is related to the input/output (I/O) interface. NAND flash typically use page-program (e.g., 4 kb per page) to achieve high bandwidth, although it has slow write time per cell. Emerging NVM macros typically do not use wide-I/O (only 64- or 128-b interface) but has fast write-time per cell. Despite the narrow I/O, the emerging NVMs remarkably improve the write/read bandwidth over the NAND or NOR flash. The data sheet of the prototype chip parameters (e.g., capacity, performance, etc.) can be accessed via the Arizona State University Memory Trend [40].

Next we will present a few representative prototypes for each emerging NVM.

STT-MRAM Prototypes

Toshiba reported a 64-Mb STT-MRAM prototype chip using a 65-nm CMOS

Different emerging NVM devices may have different application spaces in the memory hierarchy due to their unique characteristics.

process, featuring a 30-ns cycle time [41]; more recently, Toshiba reported a 1-Mb STT-MRAM prototype chip using a 65-nm CMOS process, improving the write/read cycle to 3 ns [42]. TSMC reported a 1-Mb STT-MRAM prototype chip using a 40-nm CMOS process and featuring a 10-ns read cycle time [43]. Qualcomm/TDK-Headway reported a 1-Mb STT-MRAM prototype chip using a 40-nm CMOS process, featuring a 20-ns write/read cycle time [44].

PCRAM Prototypes

Numonyx (now Micron) reported a 1-Gb 1T1R PCRAM prototype [45]. The cell selection device is a bipolar junction transistor. The fabrication was done in 45-nm process, and 9-MB/s write bandwidth and 266-MB/s read bandwidth were demonstrated. Samsung reported an 8-Gb cross-point PCRAM prototype chip [46]. The cell selection device is a silicon p-n diode. The fabrication was done in a 20-nm process. A 40-MB/s write bandwidth has been demonstrated.

RRAM Prototypes

ITRI reported a 4-Mb 1T1R HfO_x-based RRAM prototype chip [47]. The fabrication was done in a 180-nm CMOS process. A single-level-cell operation with 7.2-ns read/write random access was presented, and an MLC 2 b/cell operation with 160-ns write-verify scheme was demonstrated. Panasonic reported an 8-Mb cross-point TaO_x-based RRAM prototype chip [39]. The fabrication was done in a 180-nm CMOS process. A 443-MB/s write throughput (64-b parallel write per 17.2-ns cycle) and a 25-ns read access has been demonstrated. For the embedded applications, National Tsing-Hua University reported a 4-Mb macro in 65-nm logic-compatible process [48] and a 1-Mb macro in a 28-nm logic-compatible process [49]. For the large-capacity standalone applications, SanDisk/Toshiba reported a 32-Gb cross-point OxRAM prototype chip with a 24-nm cell half-pitch [50]. Both Panasonic and SanDisk/Toshiba's design adopted a two-layer stacked cross-point array architecture by sharing the BL to increase the integration density (similar to Intel/Micron's 3D X-point architecture [51]). Recently, Micron/Sony reported a 16-Gb 1T1R CBRAM prototype chip [52]. The fabrication was done in a 27-nm DRAM-like process. A 200-MB/s write bandwidth and 1-GB/s read bandwidth have been demonstrated.

Applications of Emerging NVM

Replacing Existing Technologies in Memory Hierarchy

Different emerging NVM devices may have different application spaces in the memory hierarchy due

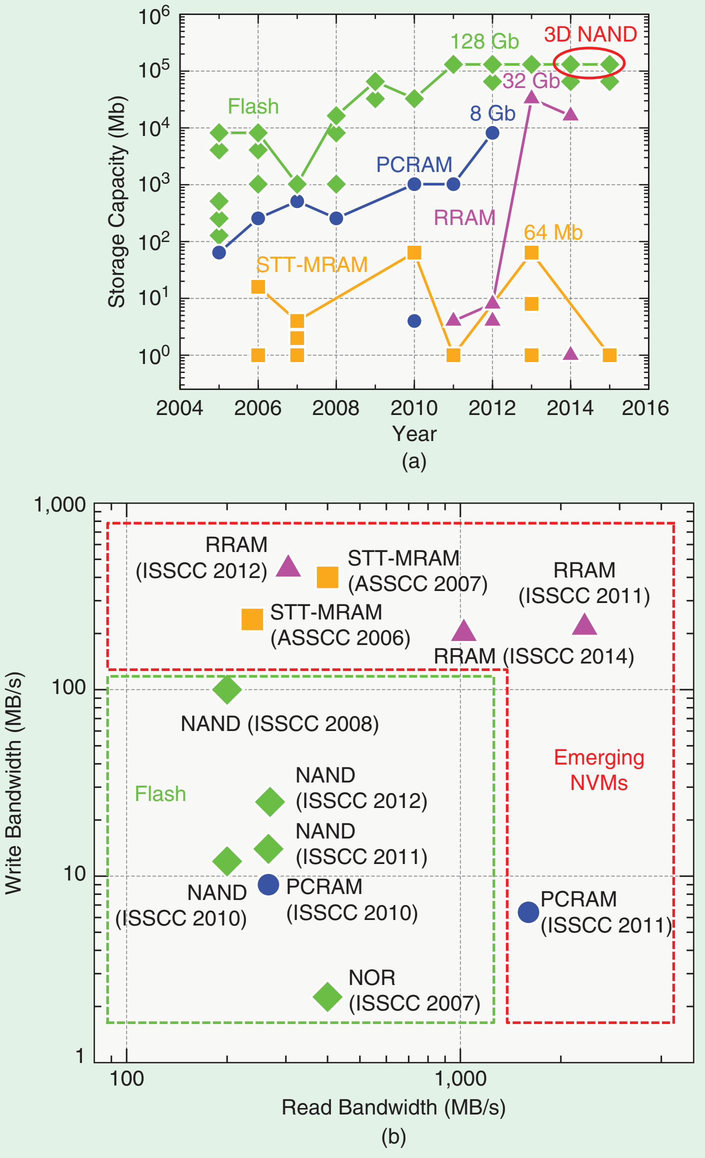

FIGURE 5: A summary of (a) memory capacity versus years and (b) write/read bandwidth versus years. The data are collected from major conferences such as IEDM, ISSCC, and VLSI from 2005 to 2015 [40].

to their unique characteristics. STT-MRAM has advantages of fast write/read speed (<10 ns) and long endurance ($>10^{15}$ cycles) that PCRAM/RRAM lacks; thus, STT-MRAM is attractive to replace SRAM or embedded DRAM in the last-level cache. Today's STT-MRAM has >30 F^2 cell area; thus it is not economically competitive to replace DRAM for main memory. In the long run, with the reduction of write current of the STT-MRAM, it may have the potential to achieve 6 F^2 cell area. Then it may become attractive to replace DRAM for main memory because it does not need the periodic refresh. On the other hand, PCRAM/RRAM has advantages of a smaller cell area (4 F^2~6 F^2) and, thus, a larger capacity than STT-MRAM; however, its endurance is typically in the range of 10^6–10^{10} cycles; thus it is more suitable for the storage-class memory filling the gap between the main memory and the storage memory (e.g., SSD). With the smart architectural wear-leveling techniques [53], the requirement of the cycling endurance for the main memory system can be reduced to 10^{10} cycles; PCRAM/RRAM may meet this requirement with the help of a strong error-correct code. It is not economically promising for PCRAM/RRAM to directly replace the NAND flash for standalone SSD due to a higher cost per bit. State-of-the-art two-dimensional (2D) NAND flash has been scaled down to around 15 nm in 2015, while the 3D stackable NAND flash is emerging [54], [55]. Twenty-four-, 32-, and 48-layer (up to 256 Gb) 3D NAND flash chips featuring MLC have been demonstrated [56]–[58]. On the market, 3D NAND flash-based SSD has been commercialized. Although at the single device level, PCRAM/RRAM outperforms NAND flash in many aspects such as faster programming speed, smaller programming voltage, and better endurance. The key challenge for PCRAM/RRAM to compete with NAND flash is the integration density or, more importantly, the cost per bit. To approach similar device density as the 3D NAND flash, a technology path toward the 3D stackable PCRAM/RRAM is required. Ultimately, the 3D stacked PCRAM/RRAM may have potential to serve as high-end enterprise SSD if cost per bit is not of the highest priority but performance is.

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3D Integration of PCRAM/RRAM

There are two monolithic 3D integration approaches for PCRAM and/or RRAM technologies: one is based on stacking the conventional horizontal cross-point array layer by layer [59], as shown in Figure 6(a), which is referred to as 3D X-point as in the Intel/Micron announcement [51]; the other is the vertical pillar structure with RRAM sandwiched between the pillar electrodes and multilayer plane electrodes [60], as shown in Figure 6(b). This vertical 3D RRAM concept is similar to today's vertical channel 3D NAND flash. Figure 6(c) shows the cross-section microscopic schematic of the vertical RRAM prototype cell [61] by cutting through one pillar electrode: the RRAM cells are formed at the sidewall of the pillar electrode and in contact with the plane electrodes (highlighted by the red-dash circle), and there is one cell at each metal layer. The fabrication cost of the first approach using the stacked horizontal cross-point array is relatively higher because the number of lithography steps increases with the number of the layers; thus, the fabrication cost remains high as the lithography step and mask are expensive.

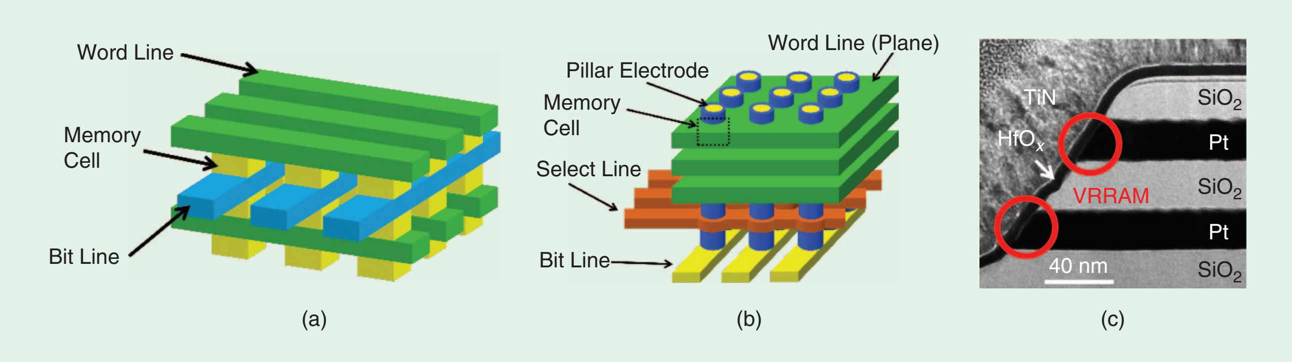

FIGURE 6: The schematics of (a) a stacked 3D horizontal cross-point array and (b) a 3D vertical cross-point array. (c) The microscopic cross section of a 3D vertical RRAM prototype by cutting through one pillar electrode. Adapted from [61].

The second approach using vertical RRAM requires only one critical lithography step to define the pillar electrodes after sequentially depositing multilayer plane electrodes, making it a more promising approach for reducing the fabrication cost. However, the cost per bit analysis for these two 3D array architectures is not sp intuitive. Although the vertical RRAM saves the fabrication cost, its minimal F is not as small as that of the horizontal counterpart; thus, it has a lower integration density because the diameter of the pillar electrode is limited by the following factors. First, the aspect ratio of the pillar electrode is limited by the etching process capability of metal/dielectric multilayers. Second, the pillar electrode resistance will drastically increase at the nanoscale. As a rough estimation, the vertical RRAM can scale to F=30 nm considering a pillar diameter (~20 nm) plus twice of the RRAM oxide thickness (~5 nm). If the horizontal RRAM can scale to F=10 nm with the help of the selector, then one layer of horizontal RRAM has the same integration density as nine layers of vertical RRAM.

A further detailed analysis is needed to assess the pros and cons of these two 3D integration approaches. The 3D horizontal cross-point array still needs the help of the selectors to address the sneak path problem as in the case of 2D cross-point array discussed earlier. The 3D vertical cross-point array prefers the built-in I–V nonlinearity of the RRAM cell as it is difficult to add the external selector on the sidewall. The problem is that the middle electrode between the selector and the RRAM cell will make a short circuit of multiple layers.

Niche Market of Emerging NVMs

Emerging NVMs may find applications in a niche market. One example is as radiation-hard NVM for aerospace electronics. Many experiments show that RRAM is robust against the radiation effects such as total ionizing dose effect [62], while the single-event-upset effect observed in the RRAM 1T1R array was attributed to the photocurrent generated at the neighboring transistor's drain to body p-n junction [63], which can be eliminated by using silicon-on-insulator transistors. Besides the standalone NVM applications, emerging NVMs are also suitable for embedded applications. RRAM devices are especially attractive due to their good compatibility with logic processes. For instance, an embedded RRAM solution has been introduced for a 28-nm technology node [64], [65]. Therefore, RRAM has great potential as MB-level embedded NVM for micro-controller applications.

Beyond the conventional memory applications, novel applications that use emerging NVM are arising.

Novel Applications of Emerging NVMs

Beyond the conventional memory applications, novel applications that use emerging NVM are arising. For instance, the use of emerging NVM as the physical unclonable function as hardware security primitive has been proposed [66], [67], which leverages the intrinsic variations in the emerging NVM's switching processes. The use of RRAM as the reconfigurable switch has also been proposed. RRAM-based FPGA was designed [68] and demonstrated [69]. The use of RRAM as ternary content-addressable-memory for fast-searching big data has been reported [70]. Adding RRAM cells on top of the SRAM cell enables the instant-on and instant-off power gating by storing data from SRAM to RRAM locally before going to standby mode, which saves the latency and power to transfer the data to off-chip or embedded flash, as shown in Figure 7. Example of nonvolatile cache include eight-transistor–two-resistor (8T2R) nonvolatile SRAM [71] and the seven-transistor–one-resistor (7T1R) nonvolatile SRAM [72]. The same principle also applies to the nonvolatile register and nonvolatile flip-flop design.

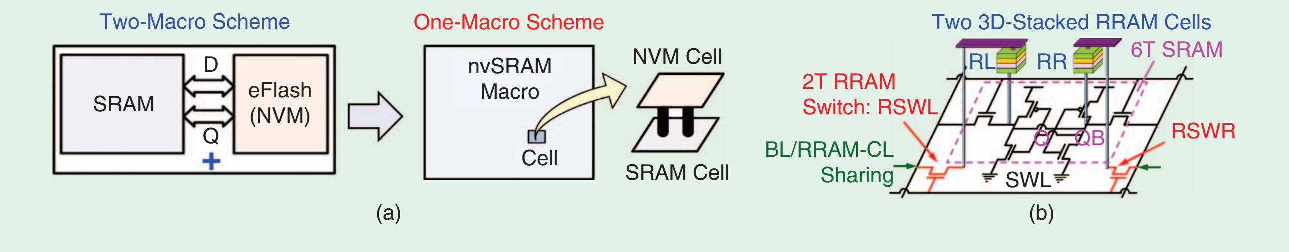

FIGURE 7: (a) Power-gating schemes: (a) two-macro with conventional embedded flash and one-macro with embedded NVM cells on top SRAM cells. (b) Eight-transistor-two-resistor (8T2R) nonvolatile SRAM. Adapted from [71].

Owing to the long endurance of STT-MRAM, it can be hybrid with logic gates (e.g., full adder or multiplier) to enable fine-grain power gating [73] and realize the logic-in-memory and eventually the nonvolatile processor. Another emerging application is using PCRAM/RRAM as synaptic devices for hardware implementation of neuro-inspired computing [74]. Owing to PCRAM/RRAM's multilevel capability, it serves as analog memory emulating the function of plastic synapses in a neural network, and the cross-point array architecture can efficiently implement the weighted sum and weight update process in the learning algorithms in an analog computing fashion [75].

Outlook

Although the early vision for emerging NVM is to replace an existing mainstream memory technology in the memory hierarchy, it is not entirely clear that these goals continue to make sense, given the many diverse potential applications of emerging NVM. By taking advantage of emerging NVM, there are enormous opportunities to completely rethink the design of the computer system to gain orders of magnitude improvement in speed and/or power consumption. Emerging NVM's unique physical properties may also add new functionality and features to the systems. A revolution of the future's computing paradigm will bring about a fundamental change in how one can extract benefits out of the technology advancements.

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